

RAICHU_SR Schematics

Stoney Ridge(FT4)

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External Net

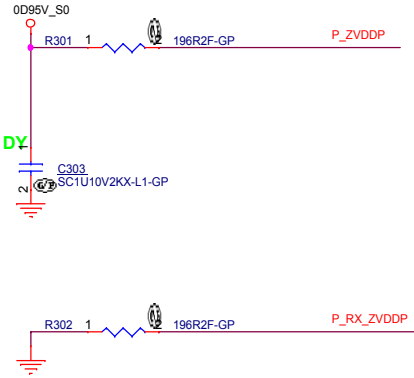
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31 LAN_PCIE_RX_P
31 LAN_PCIE_RX_N

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61 WLAN_PCIE_RX_P
61 WLAN_PCIE_RX_N

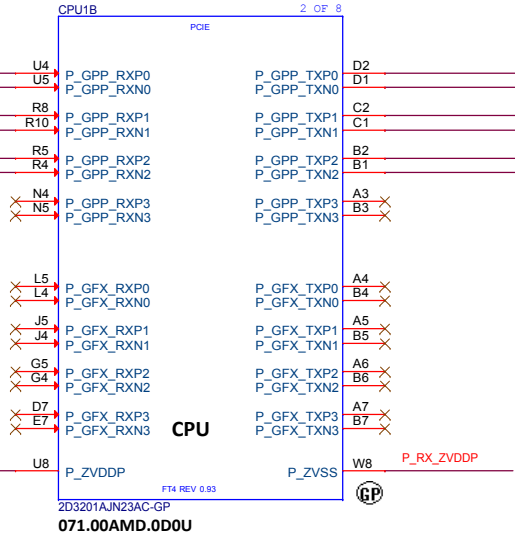
PCIe

P_GPP_CLK_port	Device	CLKREQ#
0	LAN	0
1	WIFI	1
2	EMMC	2
3	N/A	3



LAN
WIFI
EMMC

LAN_PCIE_RX_P
LAN_PCIE_RX_N
WLAN_PCIE_RX_P
WLAN_PCIE_RX_N
EMMC_PCIE_RX_P
EMMC_PCIE_RX_N



LAN
WIFI
EMMC

LAN_PCIE_TX_P
LAN_PCIE_TX_N
WLAN_PCIE_TX_P
WLAN_PCIE_TX_N
EMMC_PCIE_TX_P
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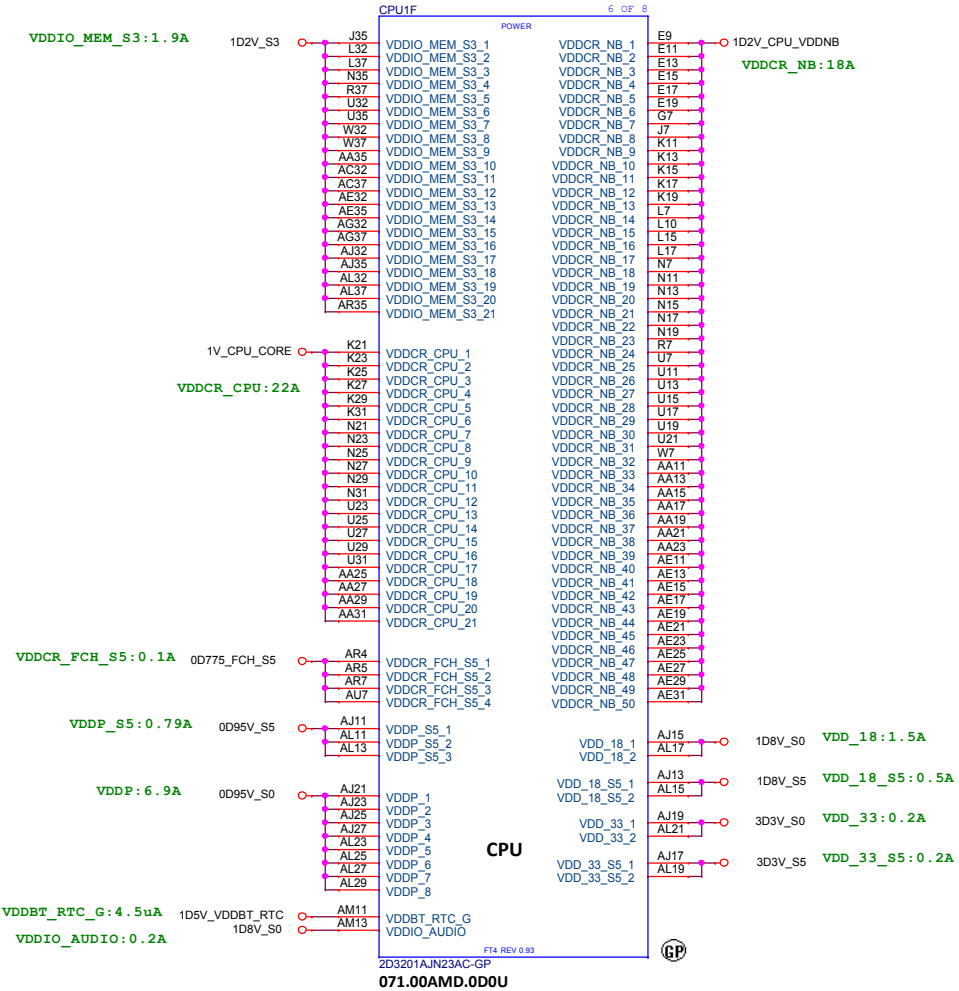
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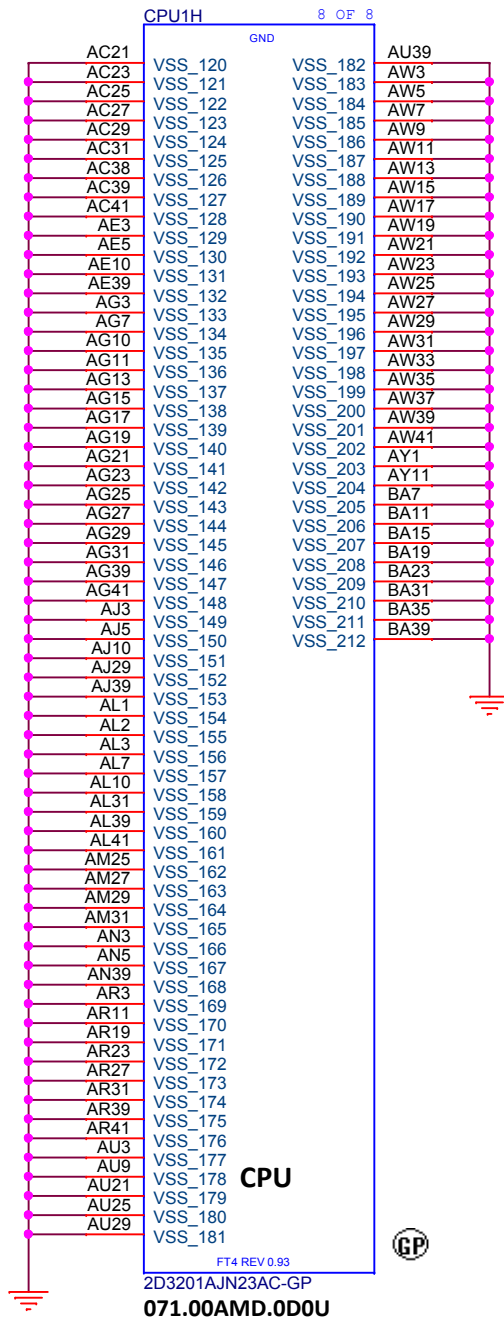
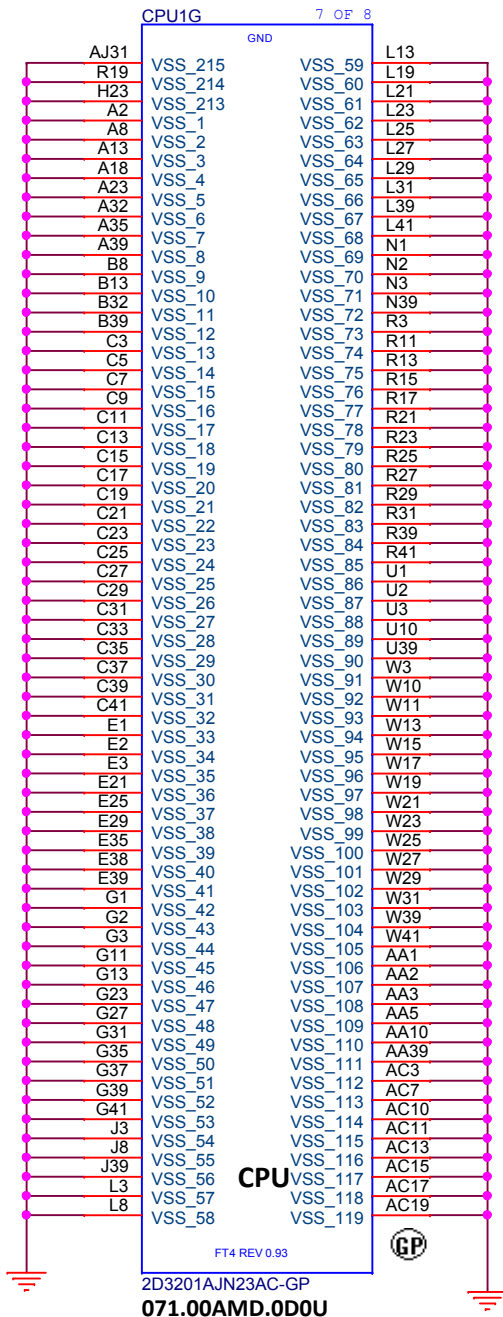
Table 4. FT4 Processor Voltage Supply Currents

Supply ¹	Nominal Voltage (V) ²	Condition	SYSTEM CONFIGURATION			
			1 (25W)	2 (15W)	3 (10W)	4 (6W)
VDDCR_CPU	Variable (0.75~1.5) ¹³	TDC ³	24	22	18	11
		EDC	32	29	24	15
		Max Loadstep ⁴	21	20	18	11
VDDCR_NB	Variable (0.75~1.2) ¹³	TDC ³	22	18	15	11
		EDC	29	24	20	15
		Max Loadstep ⁴	19	16	13	10
VDDCR_FCH_S5	0.775 ¹¹	TDC	0.1			
	Variable ¹²	TDC	0.4			
VDDIO_MEM_S3	1.50 ⁵	TDC	2.0			
	1.35 ⁶	TDC	1.9			
	1.20 ⁷	TDC	1.9			
VDDP	1.05 ⁸	TDC	7.0			
	0.95 ⁸	TDC	6.9			
VDDP_S5	1.05 ⁸	TDC	0.8			
	0.95 ⁸	TDC	0.79			
VDD_18	1.80	TDC	1.5			
VDD_18_S5	1.80	TDC	0.5			
VDD_33	3.30	TDC	0.2			
VDD_33_S5	3.30	TDC	0.2			
VDDIO_AUDIO	1.80 ⁹	TDC	0.2			
	1.50 ¹⁰	TDC	0.2			
VDDBT_RTC_G	1.50	TDC	4.5 μ A			



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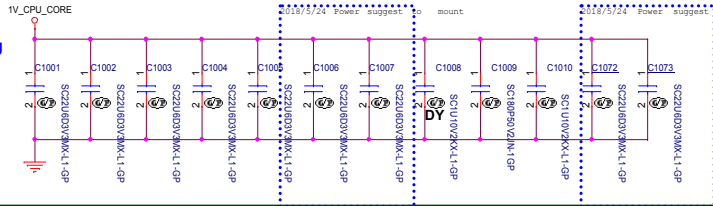
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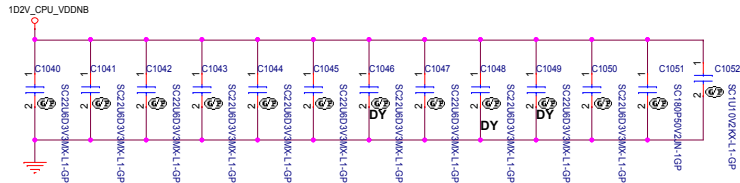
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VDDCR_CPU



VDDCR_NB



VDDIO_MEM_S3

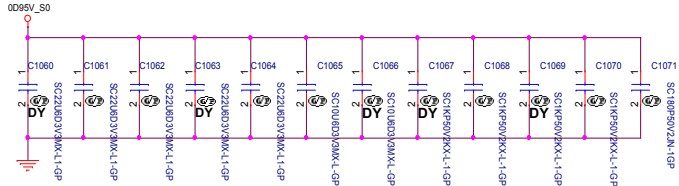
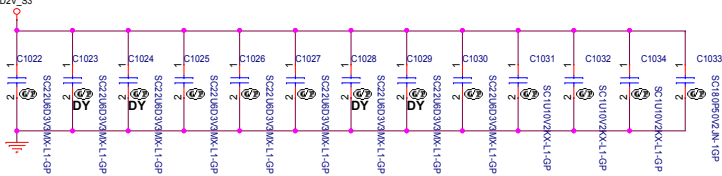


Table 169. Decoupling Capacitors for Processor Power

Capacitor		VDDCR_CPU	VDDCR_NB	VDDIO_MEM_S3 ^{1,2}	VDDCR_FCH_S5	VDDP	VDDP_S5	VDD_18	VDD_18_S5	VDD_33_S5	VDD_33	VDDIO_AUDIO	VDDRT_RTC_G
Value	Package Size / Material												
22 μ F	0603 X5R	7BU	11BU	9BU	-	5BU	-	-	-	-	-	-	-
10 μ F	0603 X5R	-	-	-	1BO	2BO	1BO	1BO	1BO	1BO	1BO	-	-
4.7 μ F	0603 X5R	-	-	-	-	-	-	-	-	-	-	-	-
1.0 μ F	0402 X5R	2BU	1BU	3BU	2BU	-	1BU	1BU	1BU	1BU	1BU	1BU	-
0.22 μ F	0402 X5R	-	-	-	-	-	-	-	-	-	-	-	-
1 nF	0402 X5R	-	-	-	2BO	4BO	1BO	1BO	1BO	1BO	1BO	2BO	1BU
180 pF	0402 COG NPO	1BU	1BU	1BU + 2(split)	-	1BO	-	-	-	-	-	-	-

Key: Capacitor locations are marked as follows:

BU = Bottom, Under the processor

BO = Bottom side, outside of the processor

T = Top, same side as the processor

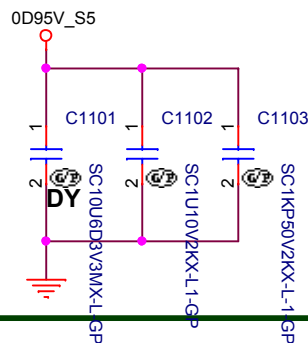
S = Close to VDDIO_MEM_S3 plane split

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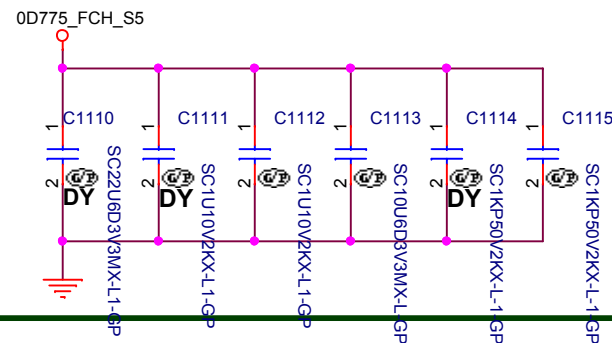
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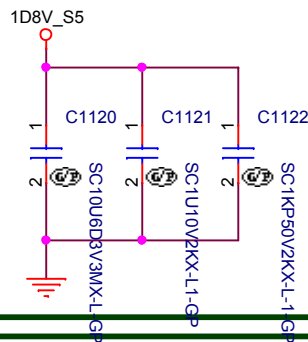
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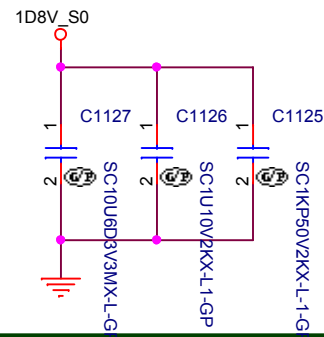
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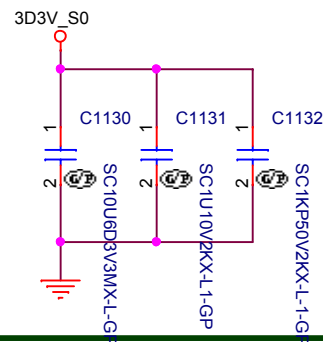
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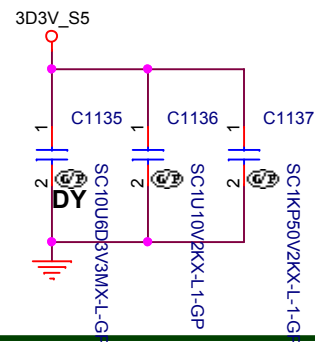
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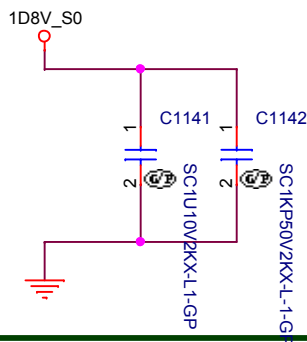
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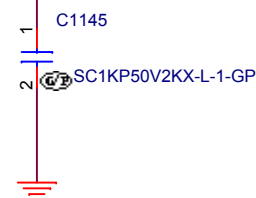
VDD_33_S5



VDDIO_AUDIO



1D5V_VDDBT_RTC



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APU FT4(Power CAP2)

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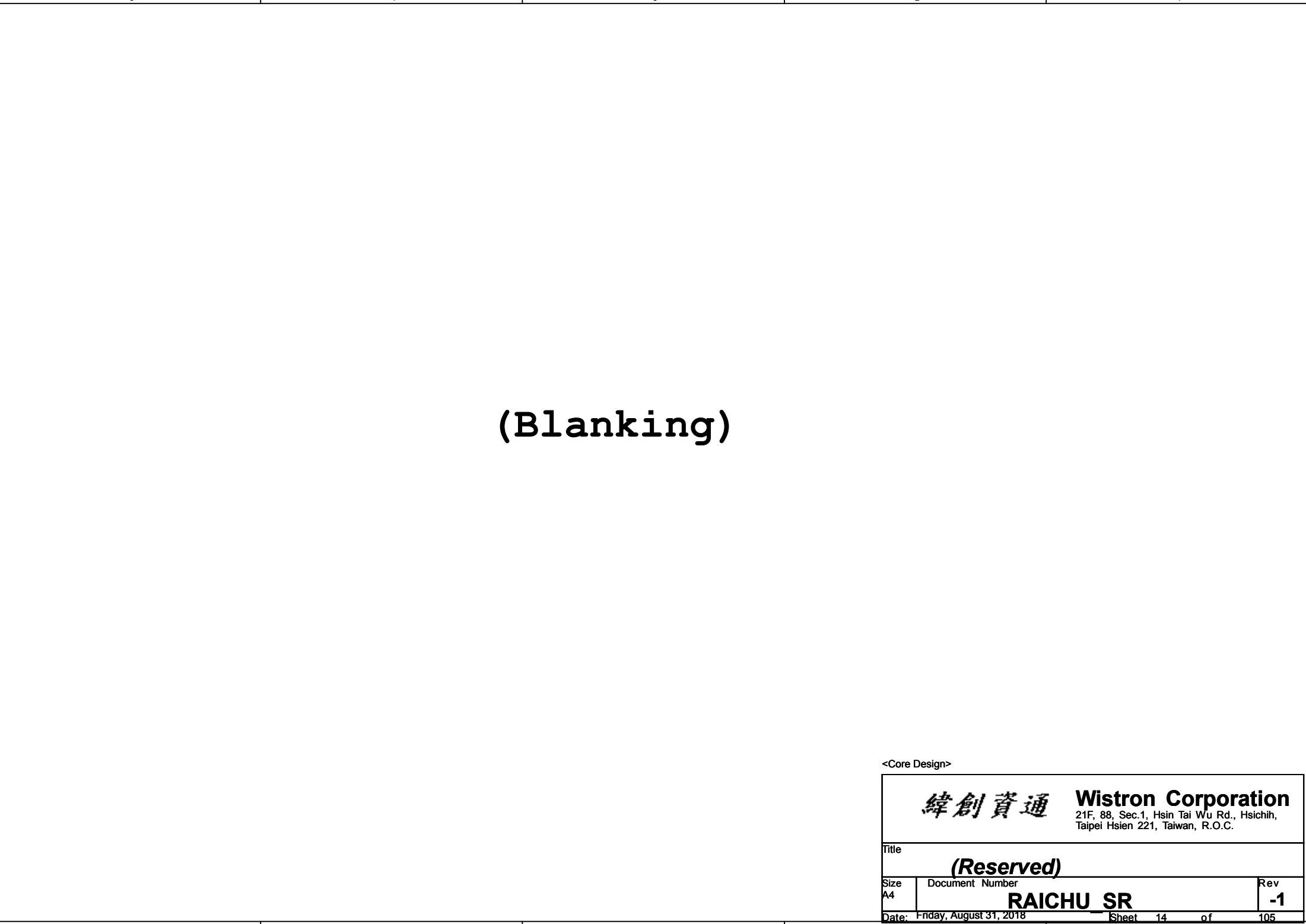
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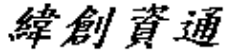
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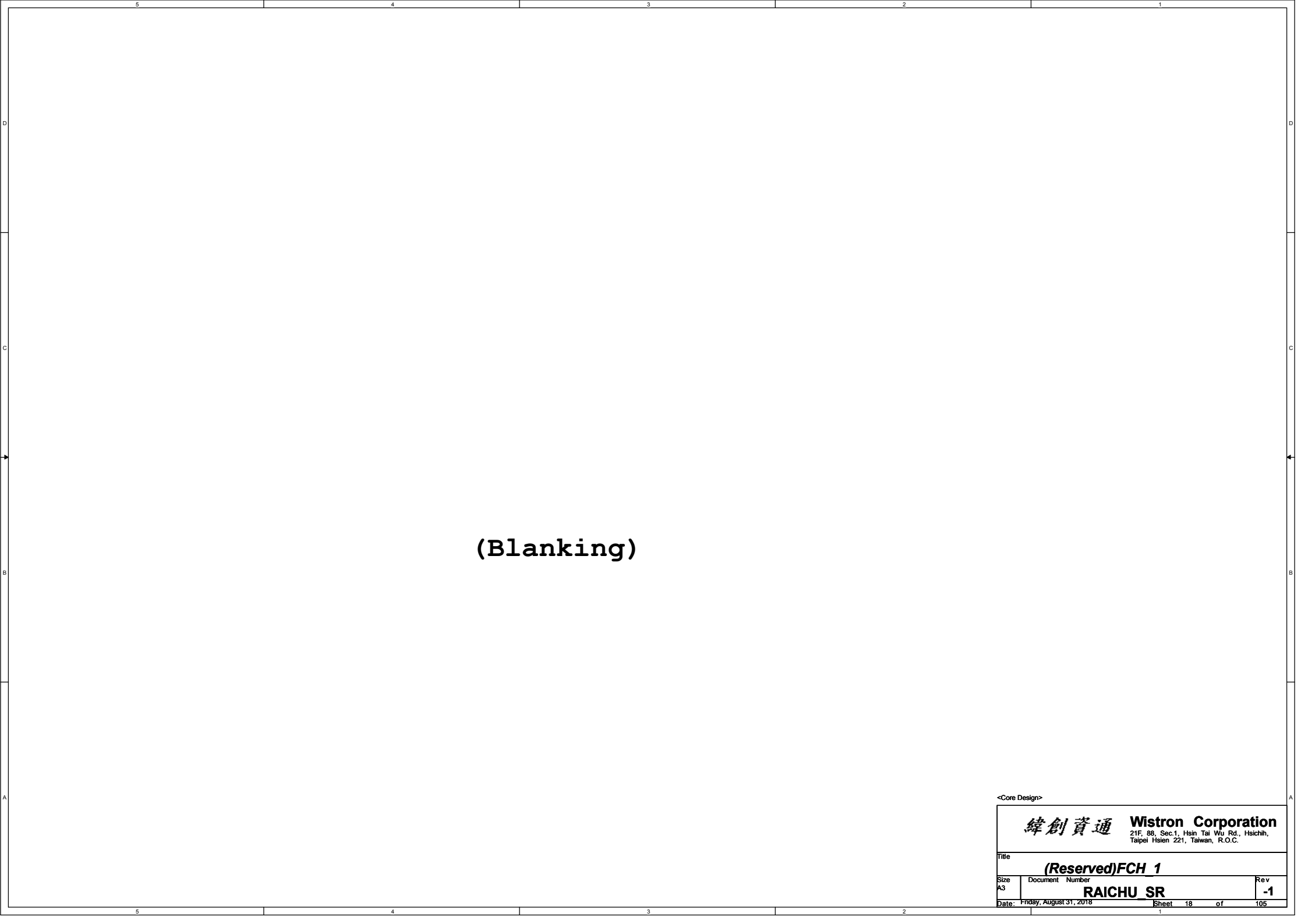
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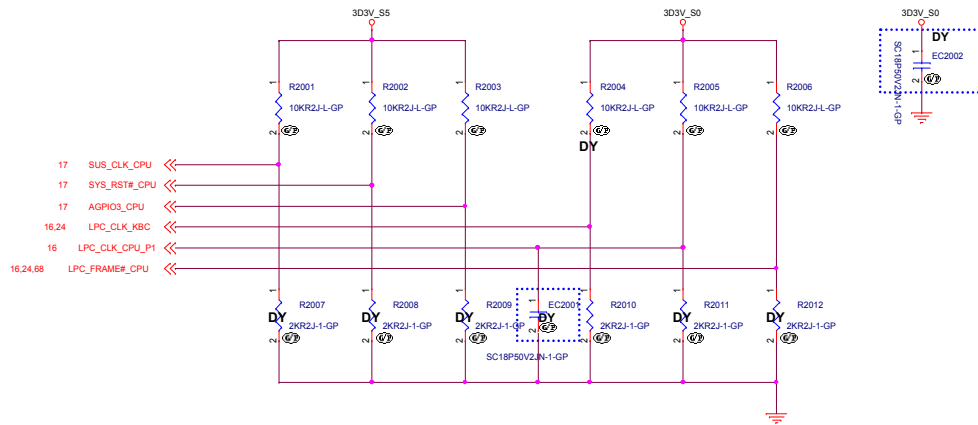
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Internal Net

External Net



REQUIRED SYSTEM STRAPS

	SUS_CLK_CPU	SYS_RST#_CPU	AGPIO3_CPU	LPC_CLK_KBC	LPC_CLK_DBG	LPC_FRAME#_CPU
Type	I	I	I	II	II	II
PULL HIGH	RTC Coin Battery is implemented DEFAULT	NORMAL_POWER_UP /RESET_TIMING DEFAULT	Enhanced Reset logic DEFAULT	Boot Fail Timer Enabled	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT
PULL LOW	RTC Coin Battery is not implemented	Reserved	Traditional Reset logic	Boot Fail Timer Disabled DEFAULT	Reserved	LPC ROM

Table 148. Strapping Options

SIGNAL Name	Strap Name	Strap Type	Default Value	Bit Value	Description			
LFRAME_L	ROMTYPE	Strap II	1	0	LPC ROM			
				1	SPI ROM 10 kΩ (± 5%) pull-up resistor to VDD_33			
LPCCLK1	CLKGEN	Strap II	1	0	Reserved			
				1	Configured for internal clock-generator 10 kΩ (± 5%) pull-up resistor to VDD_33			
LPCCLK0	BOOTFAILTIMER	Strap II	0	0	Boot Fail Timer Disabled (Default)			
				1	Boot Fail Timer Enabled 10 kΩ (± 5%) pull-up resistor to VDD_33			
RTCCLK	RTC Coin Battery	Strap I	1	0	RTC Coin Battery is not implemented			
				1	RTC Coin Battery is implemented 10 kΩ (± 5%) pull-up resistor to VDD_33_S5			
SYS_RESET_L	ShortReset	Strap I	1	0	Reserved			
				1	Normal powerup/reset timing 10 kΩ (± 5%) pull-up resistor to VDD_33_S5			
AGPIO3	Alternate Reset	Strap I	1	0	Traditional Reset logic			
				1	Enhanced Reset logic for faster resume from S5 10 kΩ (± 5%) pull-up resistor to VDD_33_S5			
Note: <ul style="list-style-type: none">To ensure Alternate Reset strap can capture correct information, platform has to make sure AGPIO3 has valid voltage config. value until 20 ms after RSMRST_L has risen to at least 3.0 v.AGPIO3 can be used as a GPIO as long as the signal is not driven on during S5 to S0 (during Resume reset time).								
Note: All strap pins must be configured with either external 10 kΩ pull-up or 2 kΩ pull-down resistors.								

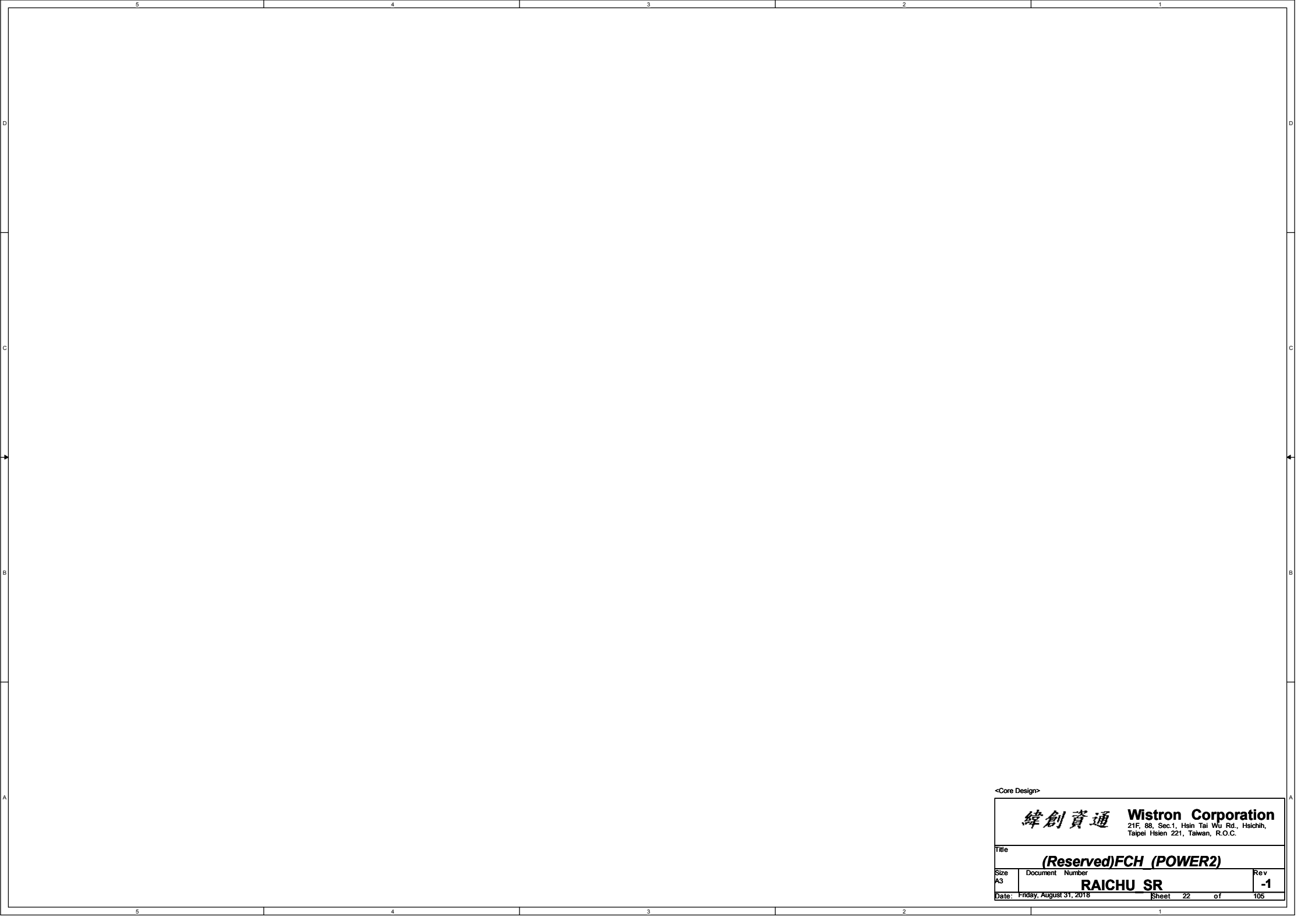
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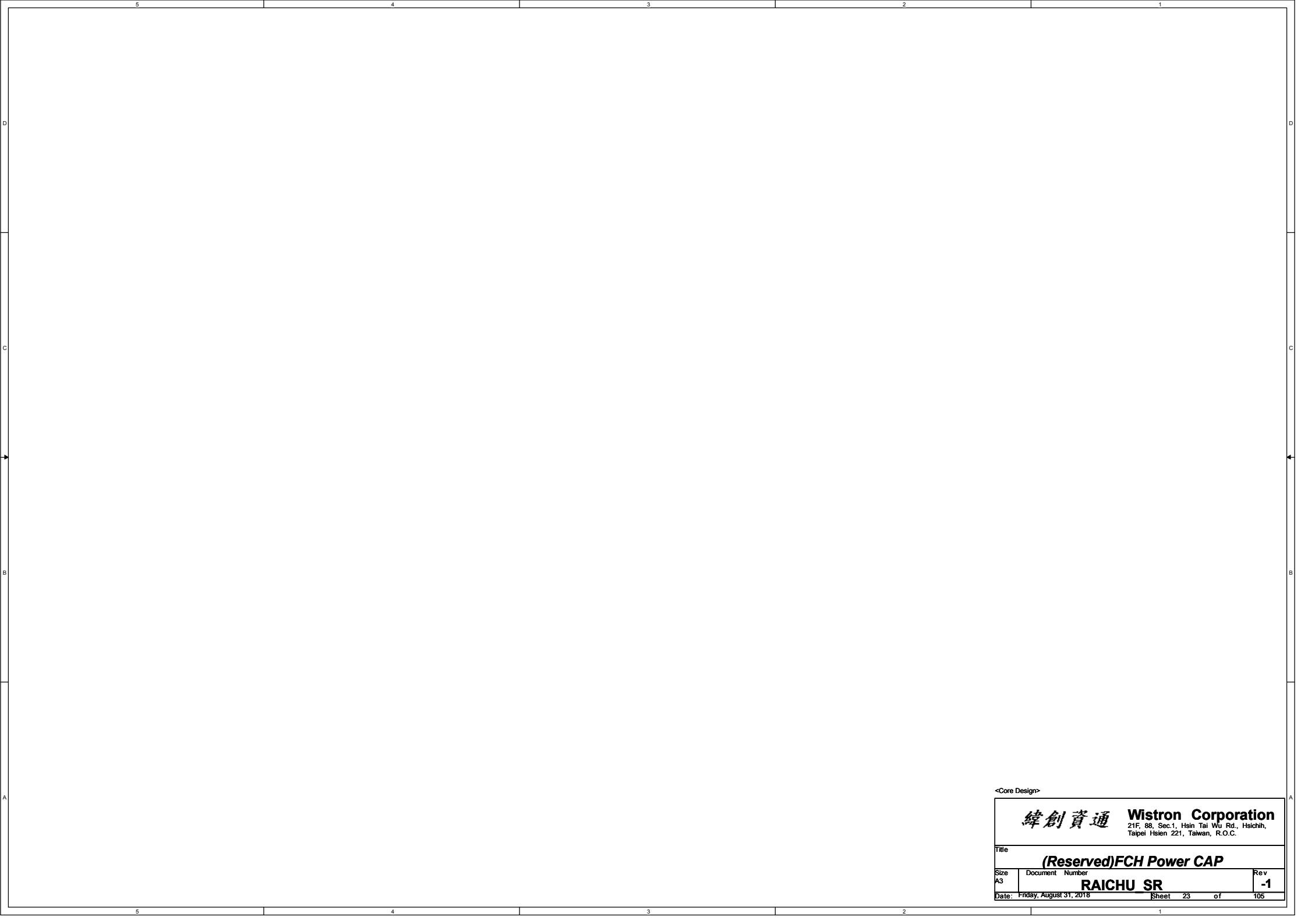
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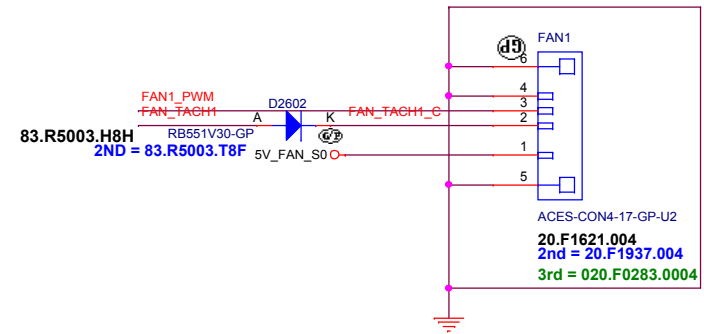
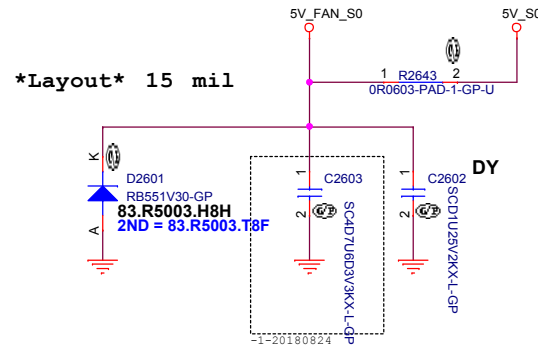
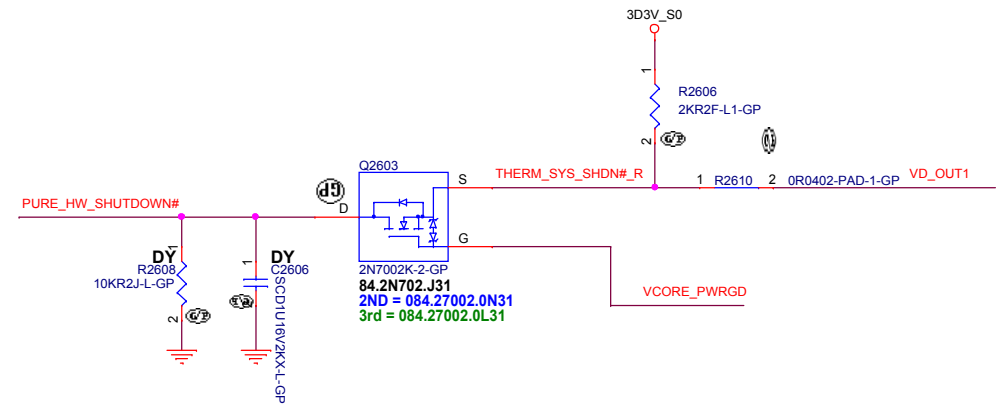
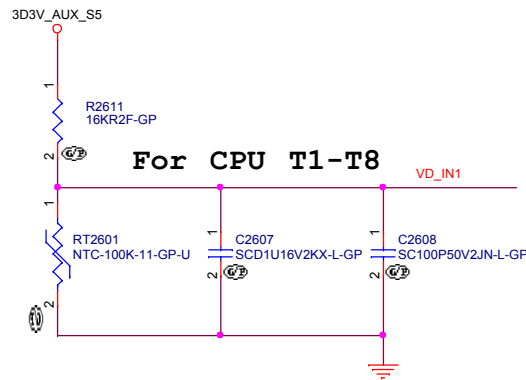
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Main Func = Thermal Sensor



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SSID = AUDIO

Speaker

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89 AUD_SPK1_L+_CON >>>
89 AUD_SPK1_R-_CON >>>
89 AUD_SPK1_R+_CON >>>

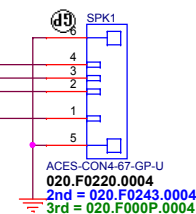
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89 AUD_HP1_JACK_L1 >>>

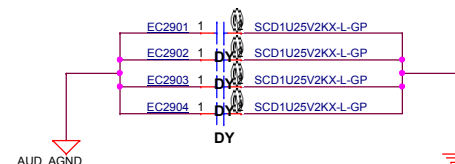
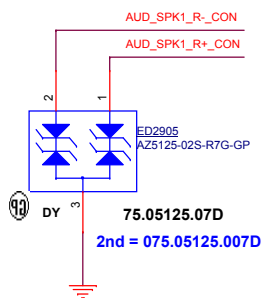
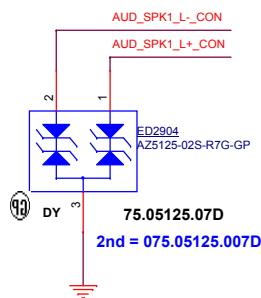
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89 AUD_HP1_ID#_TYPE >>>

AUD_SPK1_R_L-
AUD_SPK1_R_L+
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AUD_SPK1_R_R+
R2904 1 020402-PAD-1-GP
R2905 1 020402-PAD-1-GP
R2906 1 020402-PAD-1-GP
R2907 1 020402-PAD-1-GP
SB-20180712

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AUD_SPK1_R+_CON

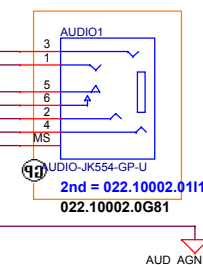


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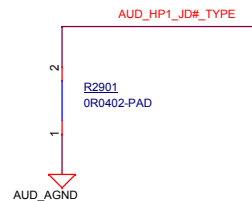
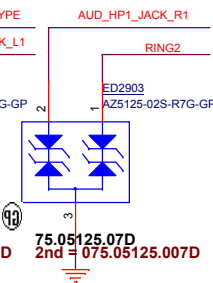
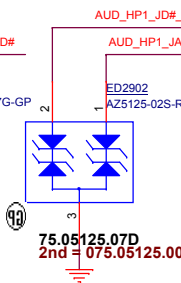
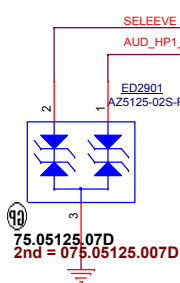


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R2902 1 63D4R3F-GP
AUD_HP1_JACK_R2
R2903 1 63D4R3F-GP
SELEEVE

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AUD_HP1_ID#_TYPE
AUD_HP1_ID#
AUD_HP1_JACK_R1



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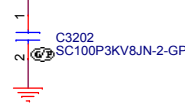
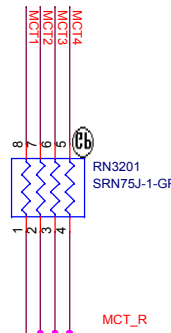
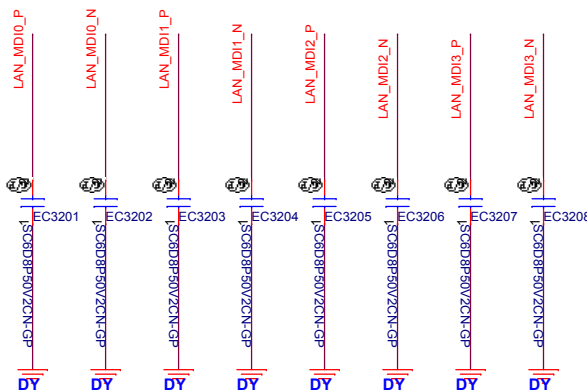
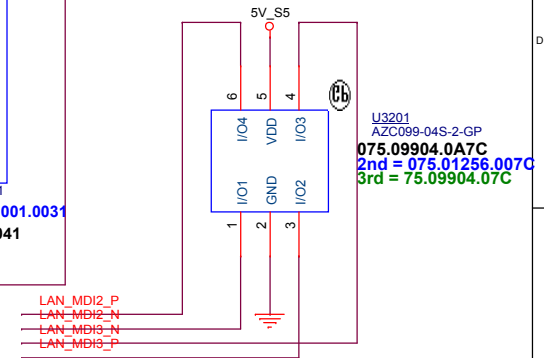
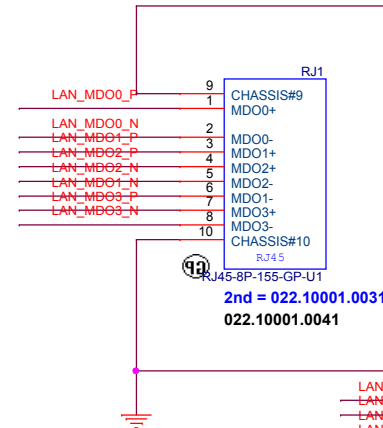
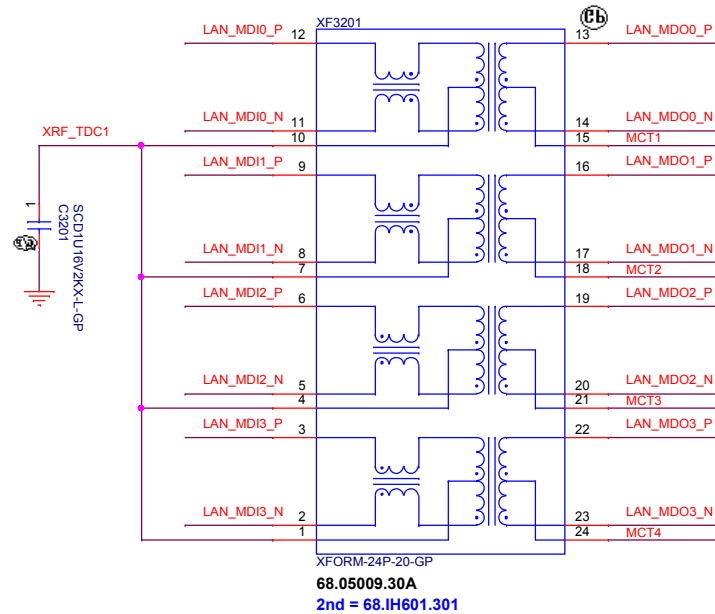
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Title <div>(Reserved)</div>		
Size <div>A4</div>	Document Number <div>RAICHU_SR</div>	Rev <div>-1</div>
Date: Friday, August 31, 2018		Sheet 30 of 106

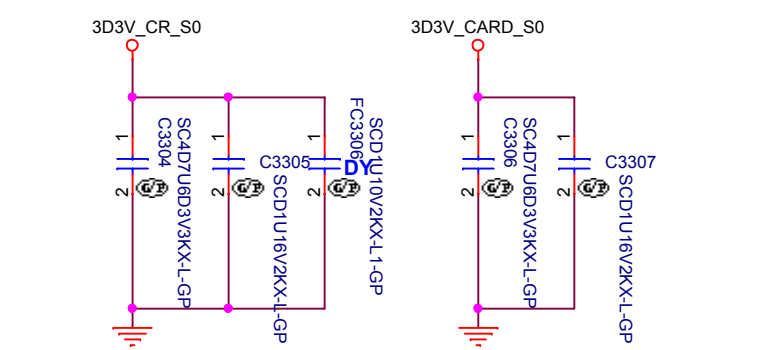
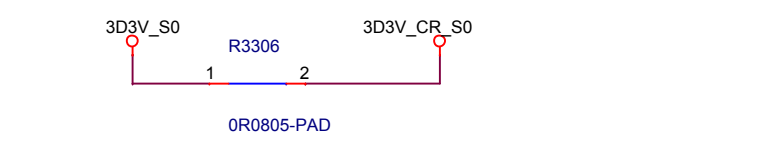
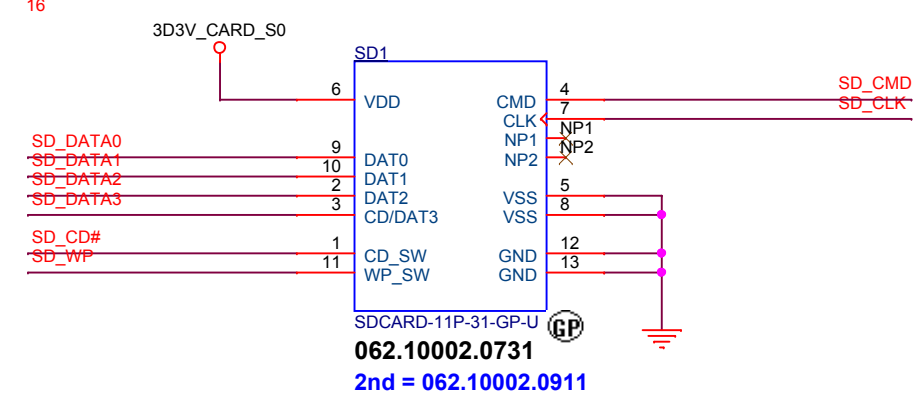
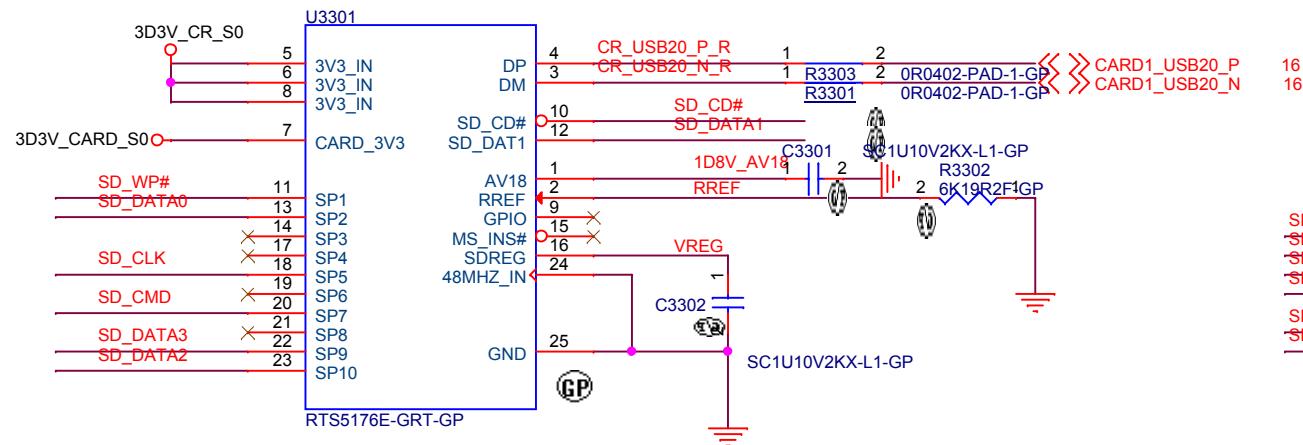
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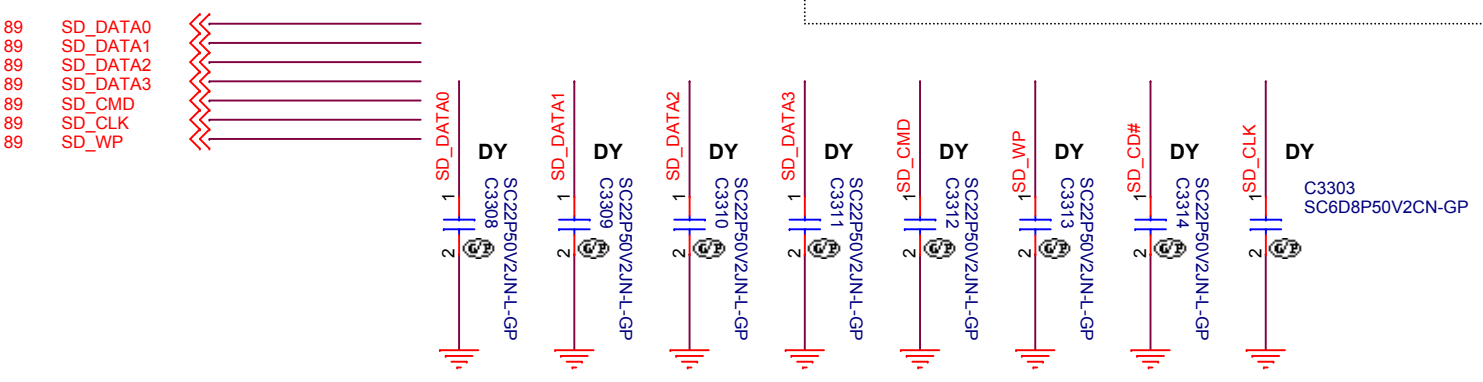
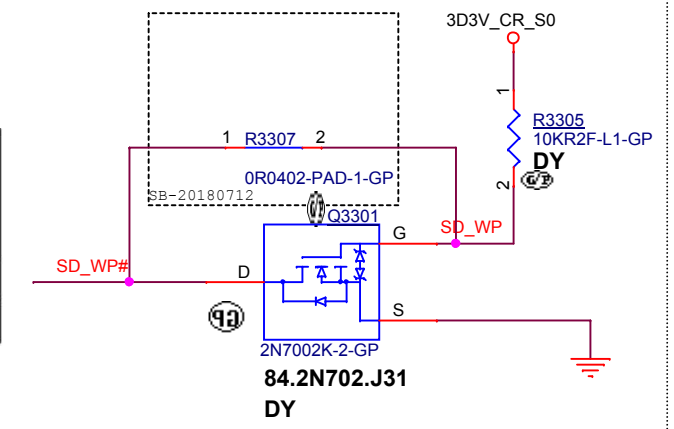
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Taipei Hsien 221, Taiwan, R.O.C.

Title			RJ45+Transformer	
Size	Document	Number	Rev	
B			-1	
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	PROTECT CONTACT		DETECT CONTACT
	WRITE PROTECT POSITION	WRITE ENABLE POSITION	
CARD UNINSERTION	OPEN	OPEN	OPEN
CARD INSERTION	OPEN	CLOSE	CLOSE



<Core Design>

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Title: **Card Reader**

Size: Document Number: **RAICHU_SR** Rev: **-1**

Date: Friday, August 31, 2018 Sheet 33 of 106

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Title <div>USB (RSVD)</div>		
Size <div>A4</div>	Document Number <div>RAICHU_SR</div>	Rev <div>-1</div>
Date: Friday, August 31, 2018		Sheet 34 of 106

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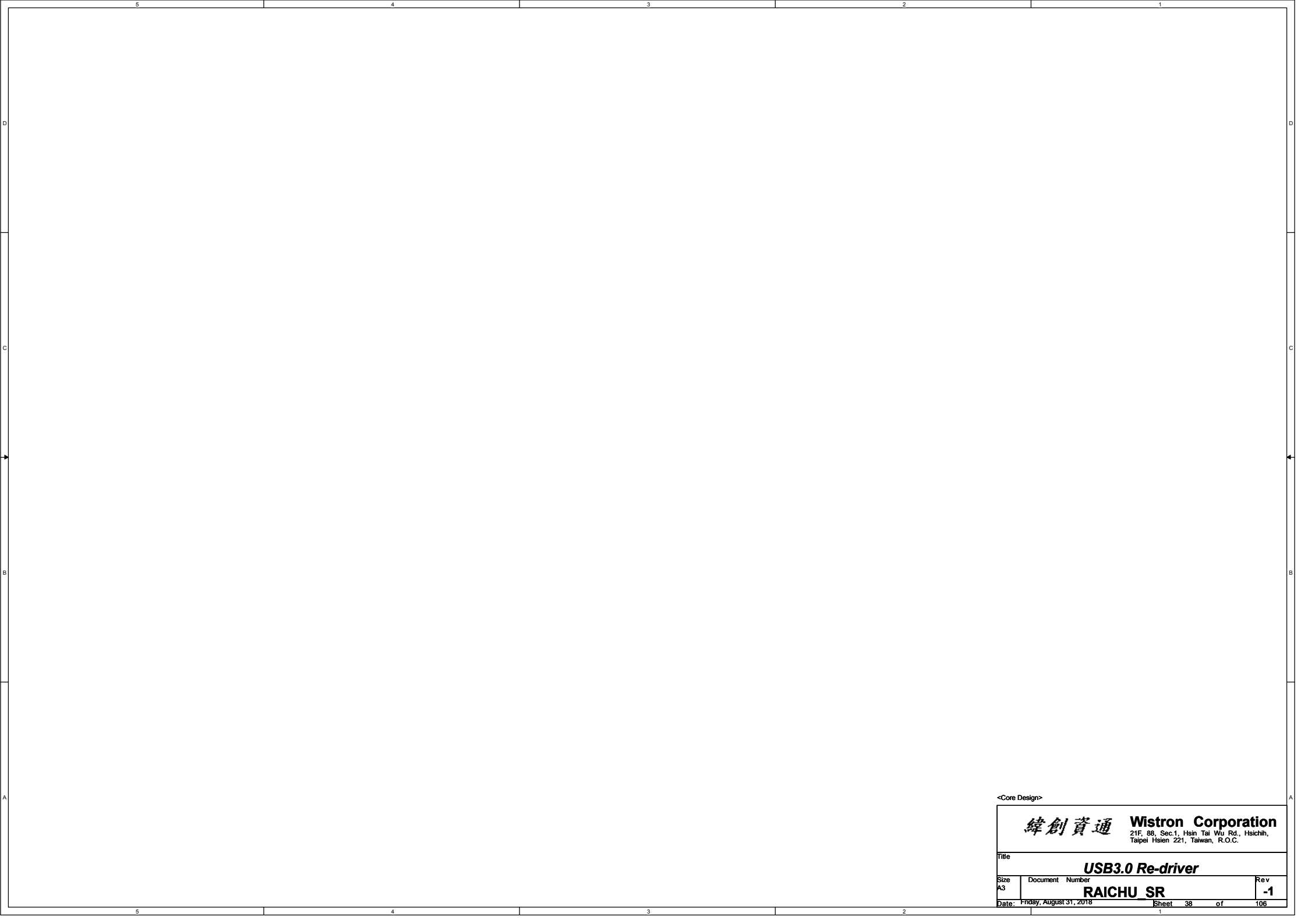
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Title <div>USB (RSVD)</div>		
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Title <div>USB (RSVD)</div>		
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Title			
USB3.0 Re-driver			
Size A3	Document Number	Rev -1	
RAICHU SR			
Date: Friday, August 31, 2018		Sheet 38 of	106

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number RAICHU_SR		Rev -1
Date:	Friday, August 31, 2018	Sheet 39 of	106

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Title <div>(Reserved)DS3</div>		
Size <div>A4</div>	Document Number <div>RAICHU_SR</div>	Rev <div>-1</div>
Date: Friday, August 31, 2018		Sheet 41 of 106

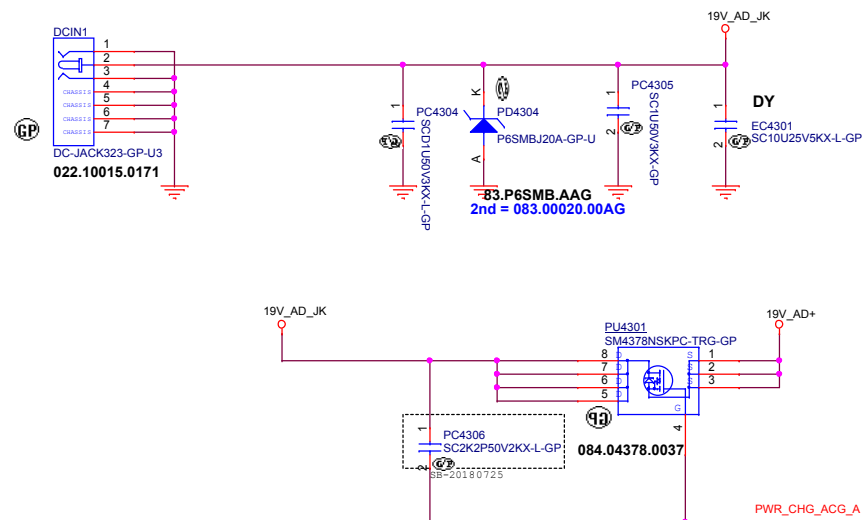
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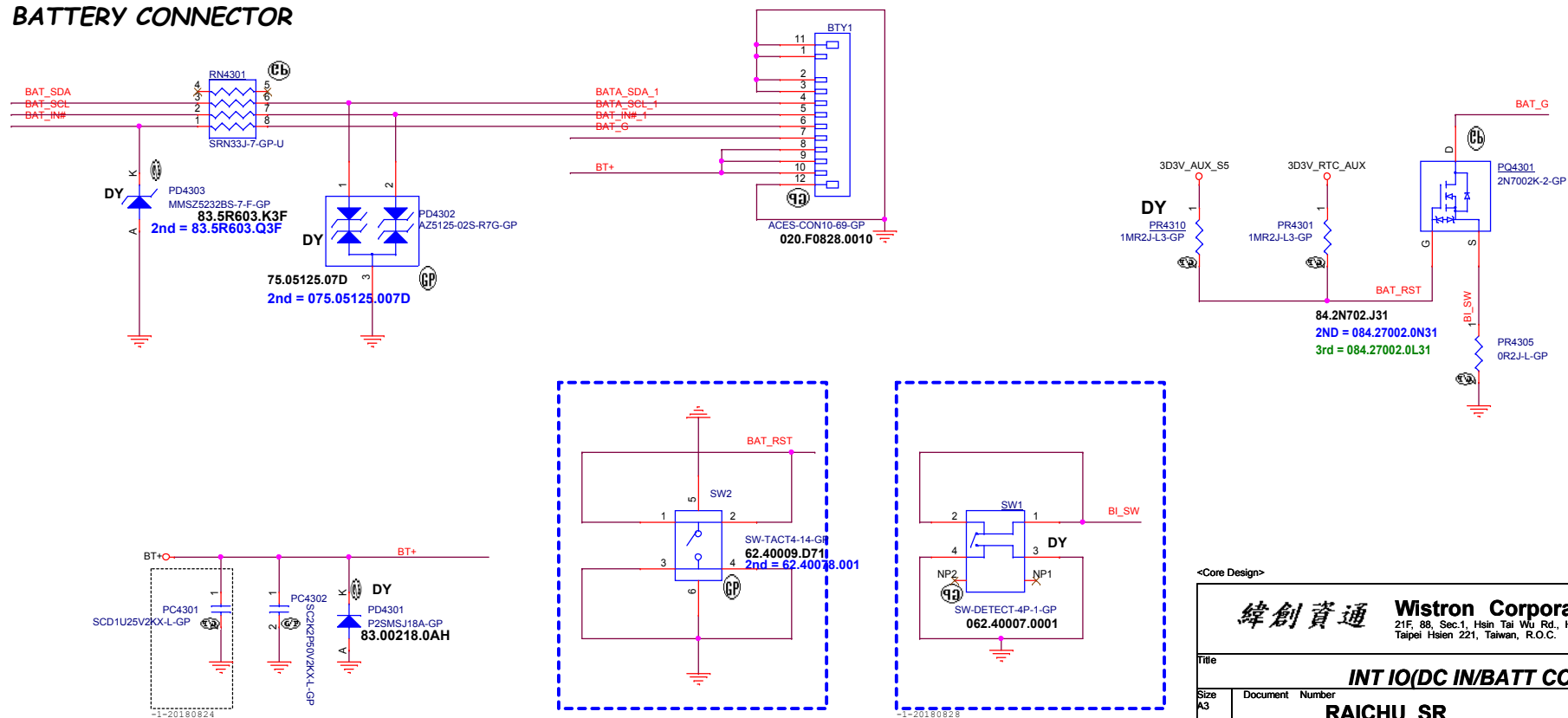
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Title (Reserved)		
Size A4	Document Number RAICHU_SR	Rev -1
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ANNIE solution

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



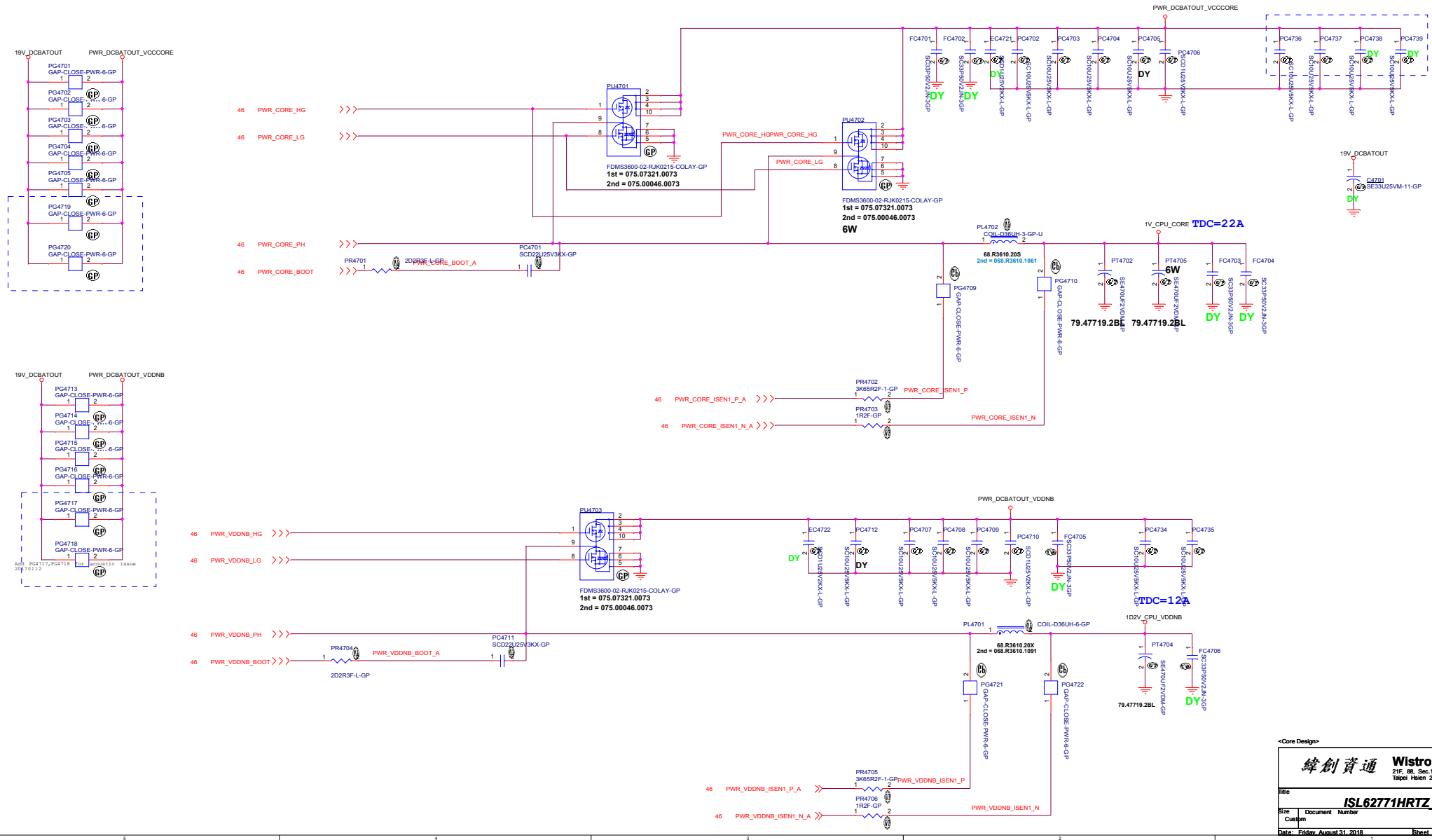
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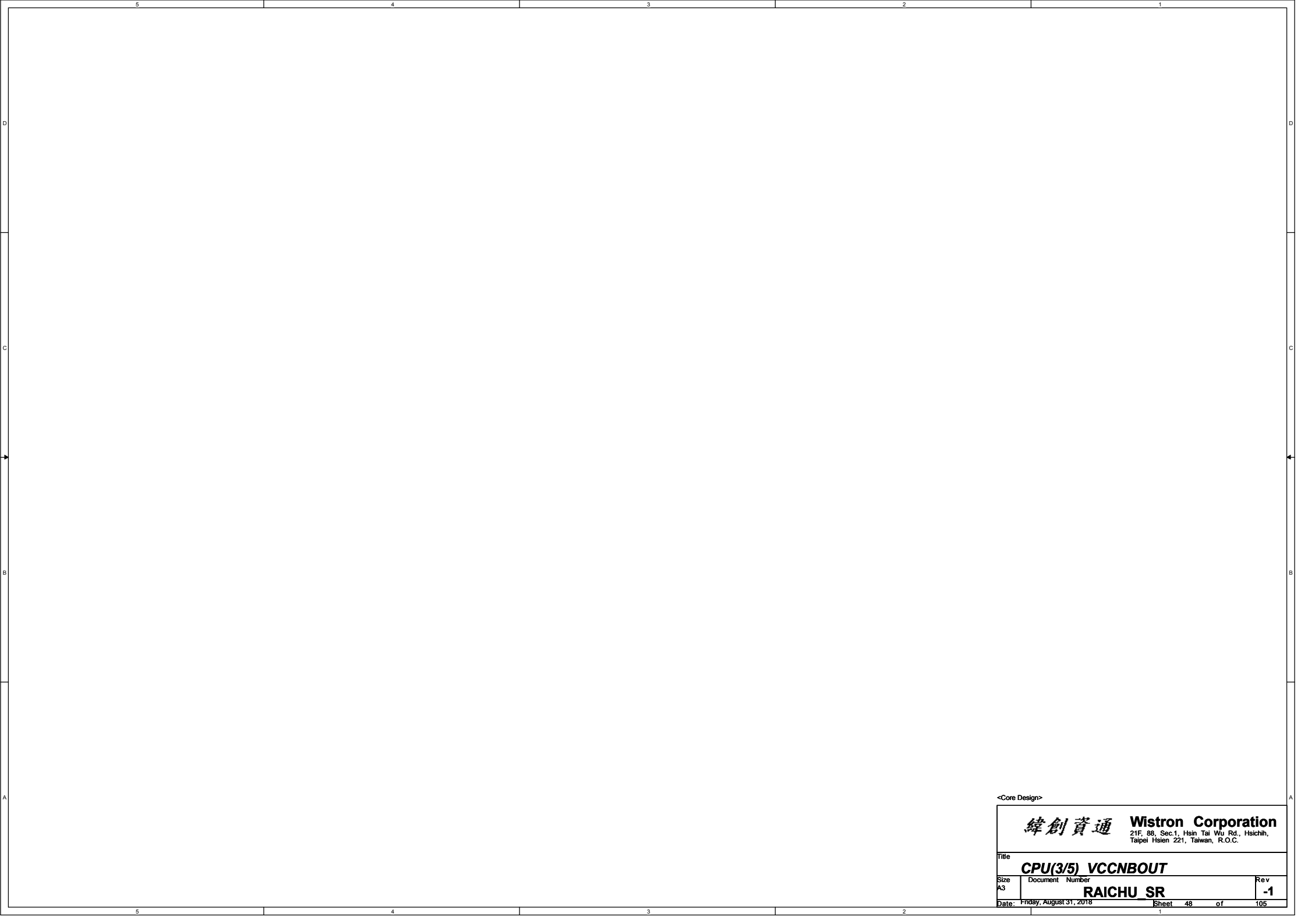
緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
INT IO(DC IN/BATT CONN)			
Size	Document Number	Rev	
A3	RAICHU SR	-1	
Date: Friday, August 31, 2018		Sheet 43	of 106

PC4738, PC4739 For acoustic debug only, can NOT be installed.
20170112





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Title			
CPU(3/5) VCCNBOUT			
Size	Document	Number	Rev
A3	RAICHU SR		-1
Date:	Friday, August 31, 2018		
		Sheet	48 of 105

40 0D775V_S5_EN <<



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

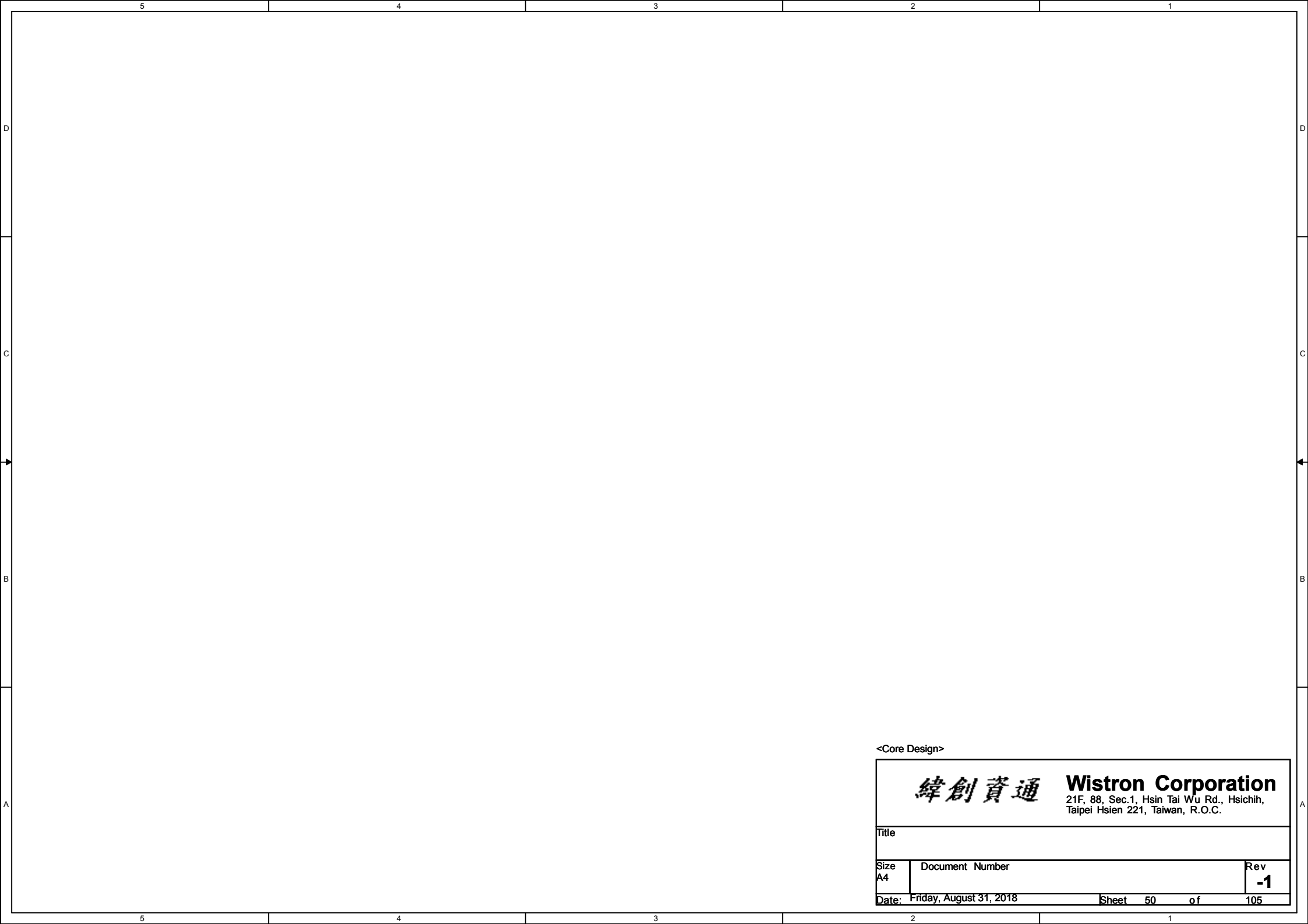
Size
A4

Document Number

Rev	-1
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Date: Friday, August 31, 2018

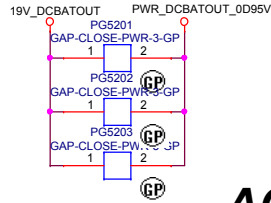
Sheet 49 of 105



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Title	
Size A4	Document Number
Date: Friday, August 31, 2018	Rev -1
Sheet 50 of 105	

SSID = PWR.Plane.Regulator_1p0v

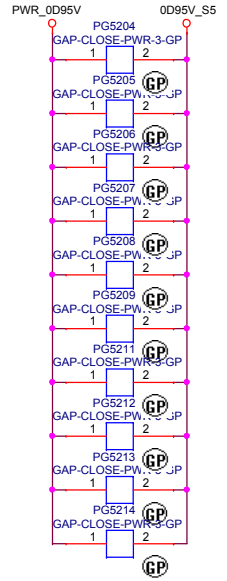
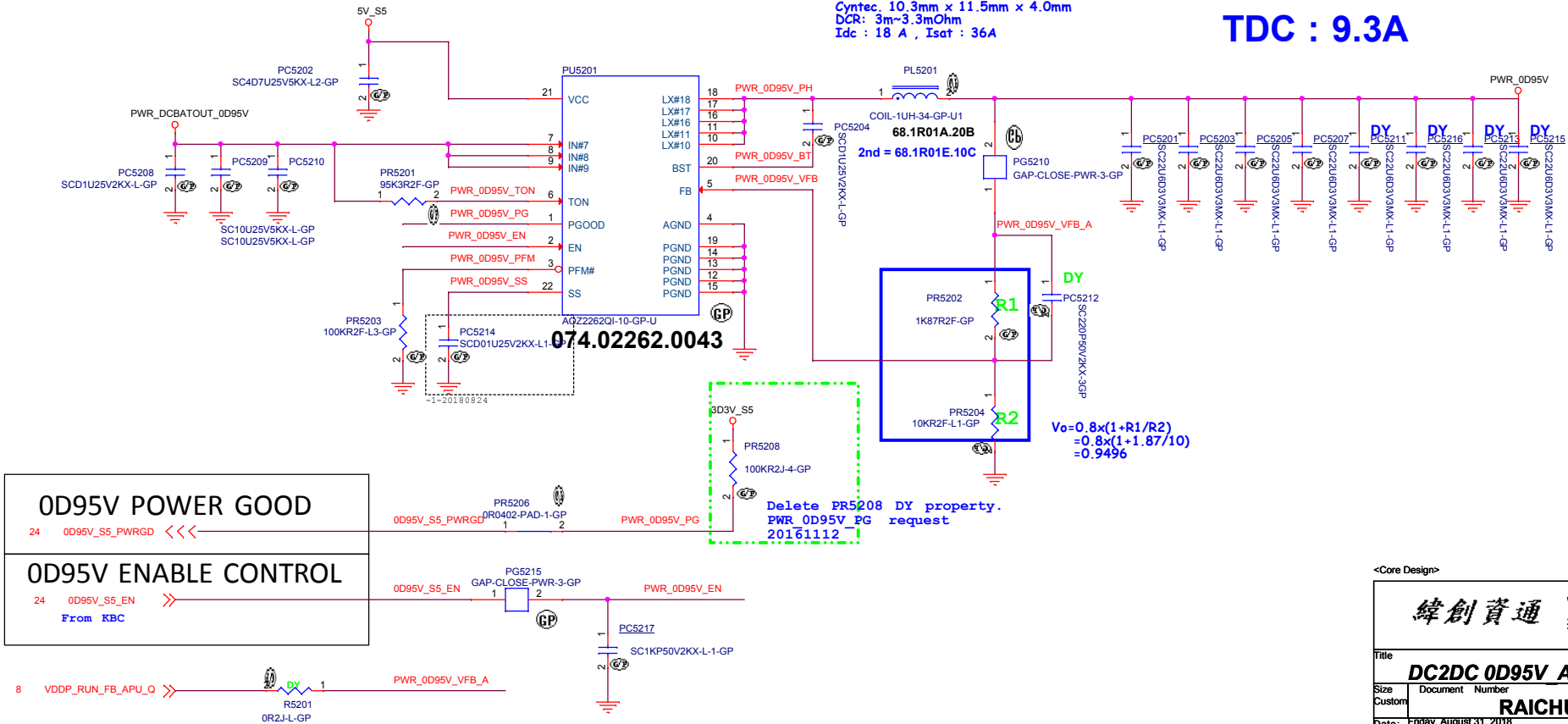


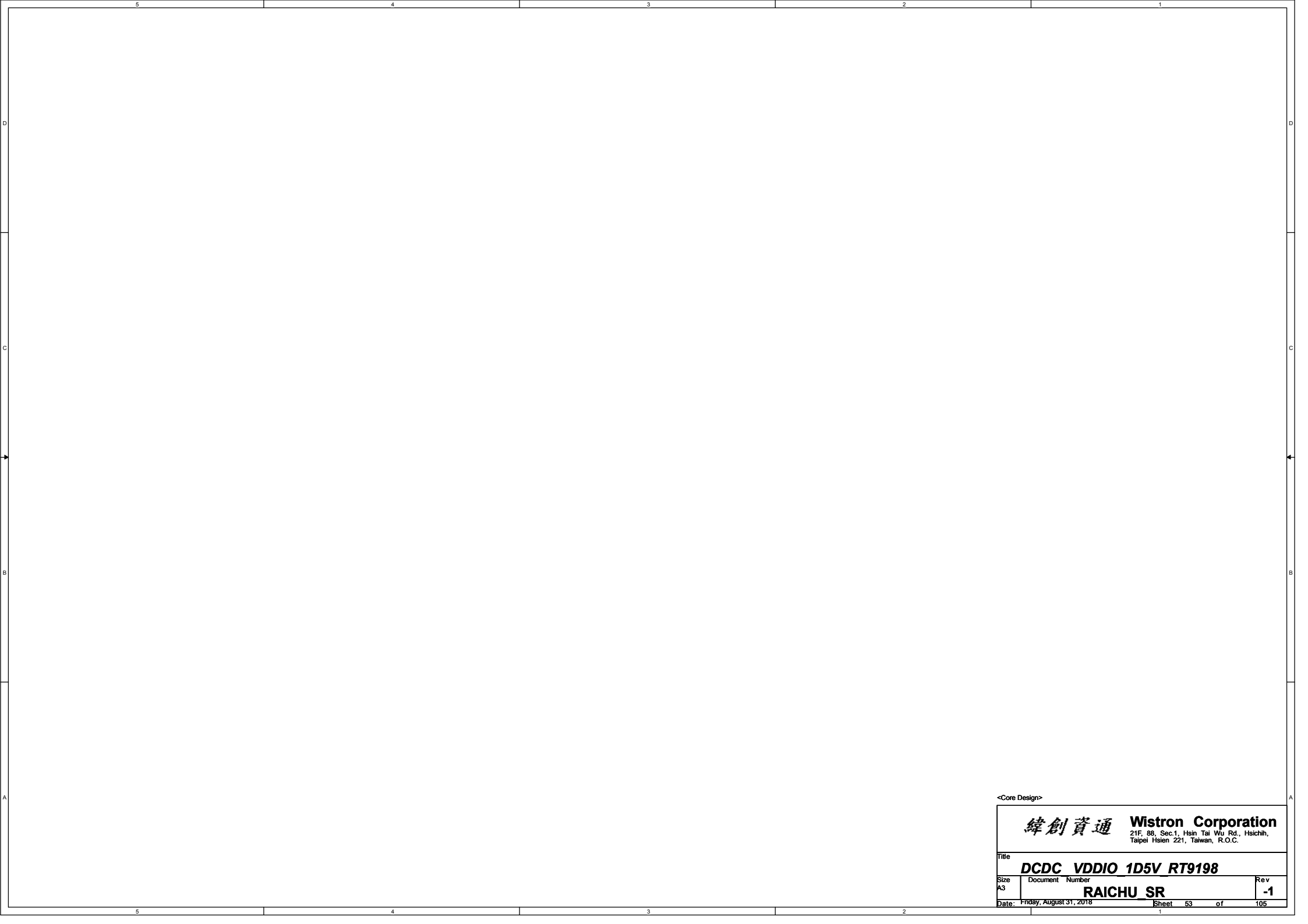
AOZ2262 for 0D95V 20161005 Power Team

IC	AOZ2262 (10A)	AOZ2261 (8A)	AOZ2260 (6A)
COM			
Chock	068.1R010.2121 IDC : 18A	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A
Output CAP	22uF/6.3V * 5pcs DY*1	22uF/6.3V * 4pcs DY*1	22uF/6.3V * 4pcs DY*1

TDC : 9.3A

Cyntec. 10.3mm x 11.5mm x 4.0mm
DCR: 3m~3.3mOhm
Idc : 18 A , Isat : 36A

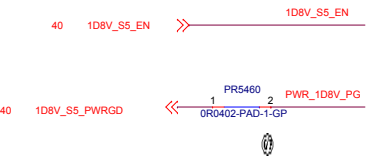




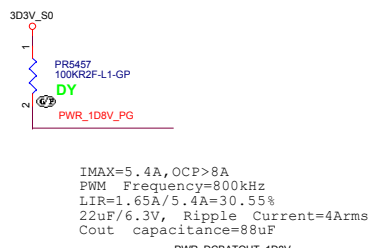
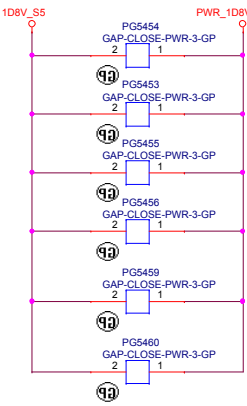
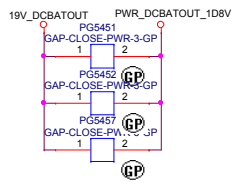
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Title		DCDC VDDIO 1D5V RT9198	
Size	Document	Number	Rev
A3	RAICHU SR		-1
Date:	Friday, August 31, 2018		Sheet 53 of 105

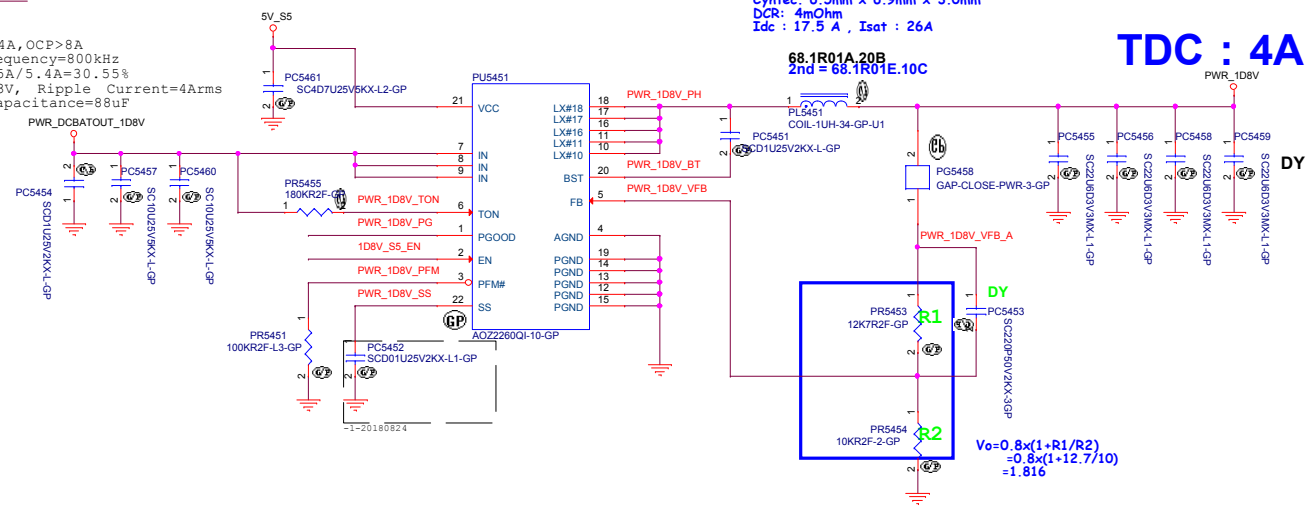
OFFPAGE



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IMAX=5.4A, OCP>8A
PWM Frequency=800kHz
LIR=1.65A/5.4A=30.55%
22uF/6.3V, Ripple Current=4Arms
Cout capacitance=88uF



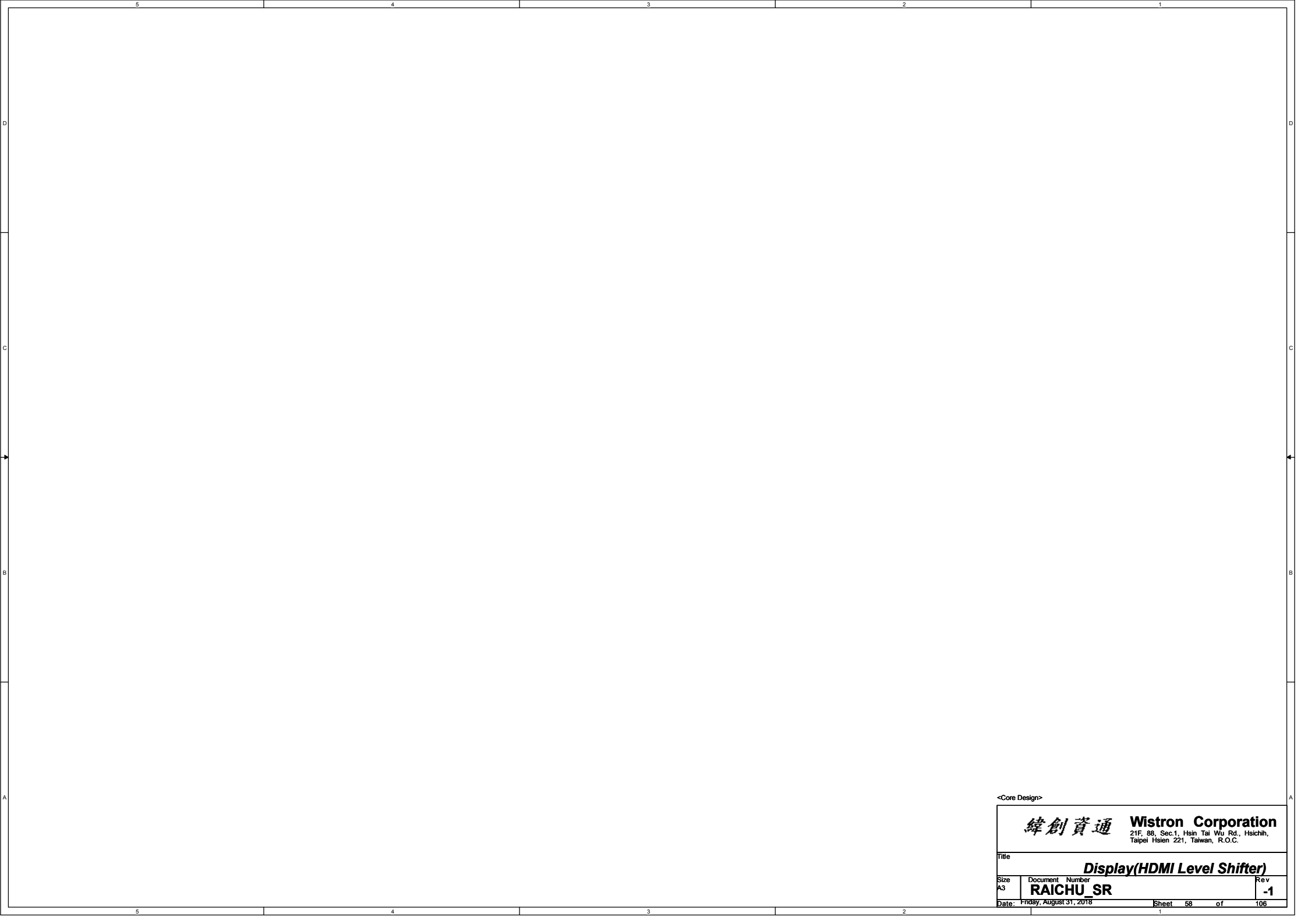
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Title: **DCDC 1D8V RT5797ALGQW**

Size: Custom Document Number: **RAICHU_SR** Rev: **-1**

Date: Friday, August 31, 2018 Sheet: 54 of 105



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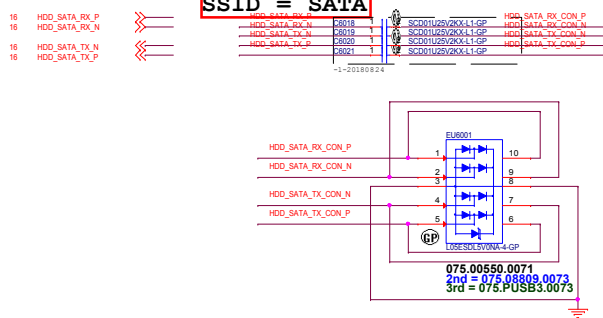
<div>緯創資通</div>		<div>Wistron Corporation</div>	
<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>			
<div>Title</div>			
<div>Display(HDMI Level Shifter)</div>			
<div>Size</div>	<div>Document Number</div>	<div>Rev</div>	
<div>A3</div>	<div>RAICHU SR</div>	<div>-1</div>	
<div>Date: Friday, August 31, 2018</div>	<div>Sheet 58 of 106</div>		

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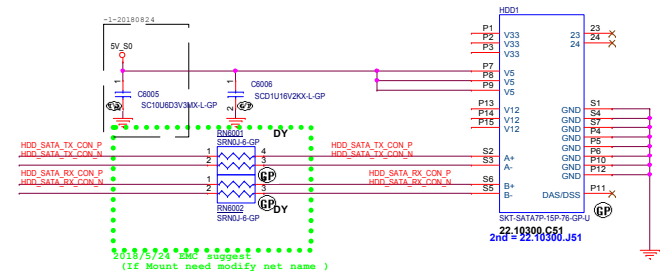
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Title <div>(Reserved)</div>		
Size <div>A4</div>	Document Number <div>RAICHU_SR</div>	Rev <div>-1</div>
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SSID = SATA



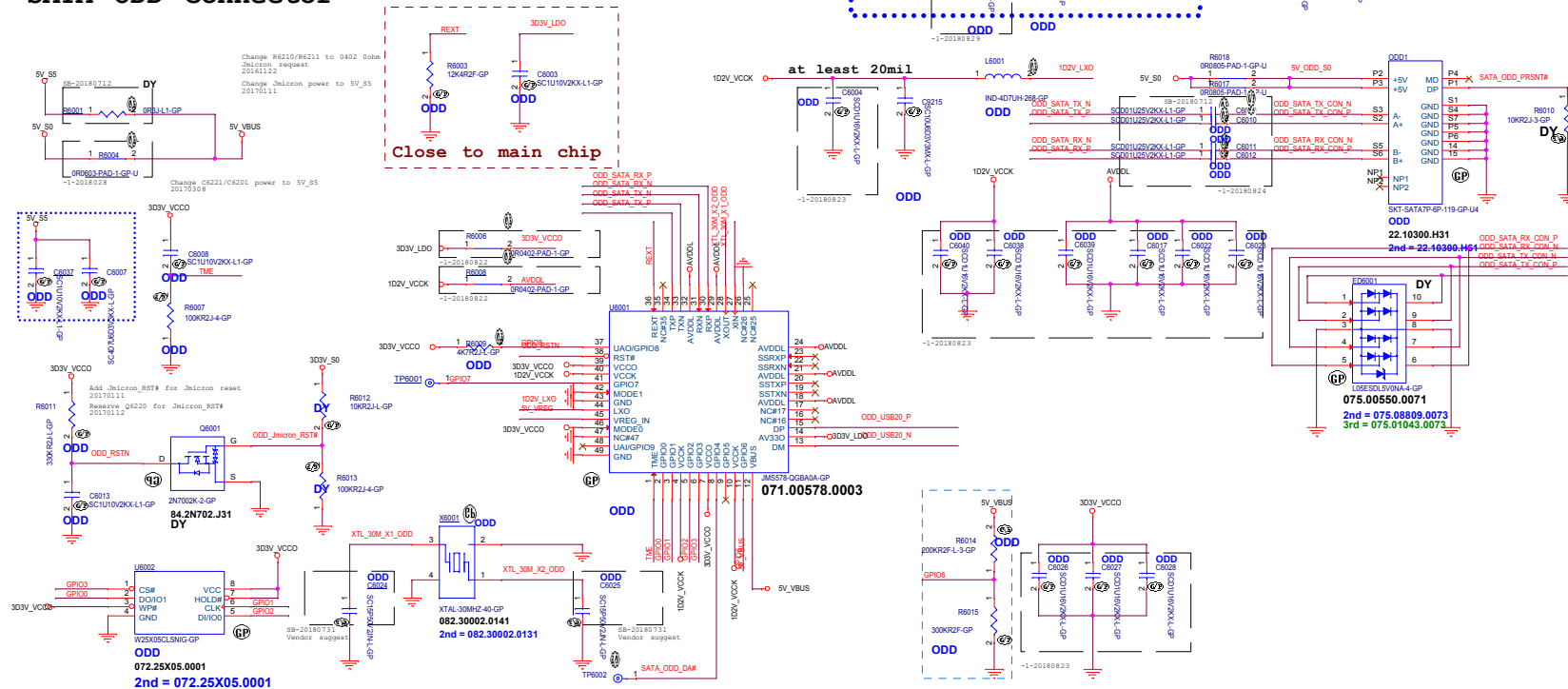
SATA HDD Connector



6.1 PCB layout guidelines :

1. Route high speed switching node LXO away from sensitive analog area (as crystal, REXT ... etc)
2. Connect input/output capacitors to power and ground plane and put input/output capacitors close to IC and keep the high-current paths as short and wide as possible.

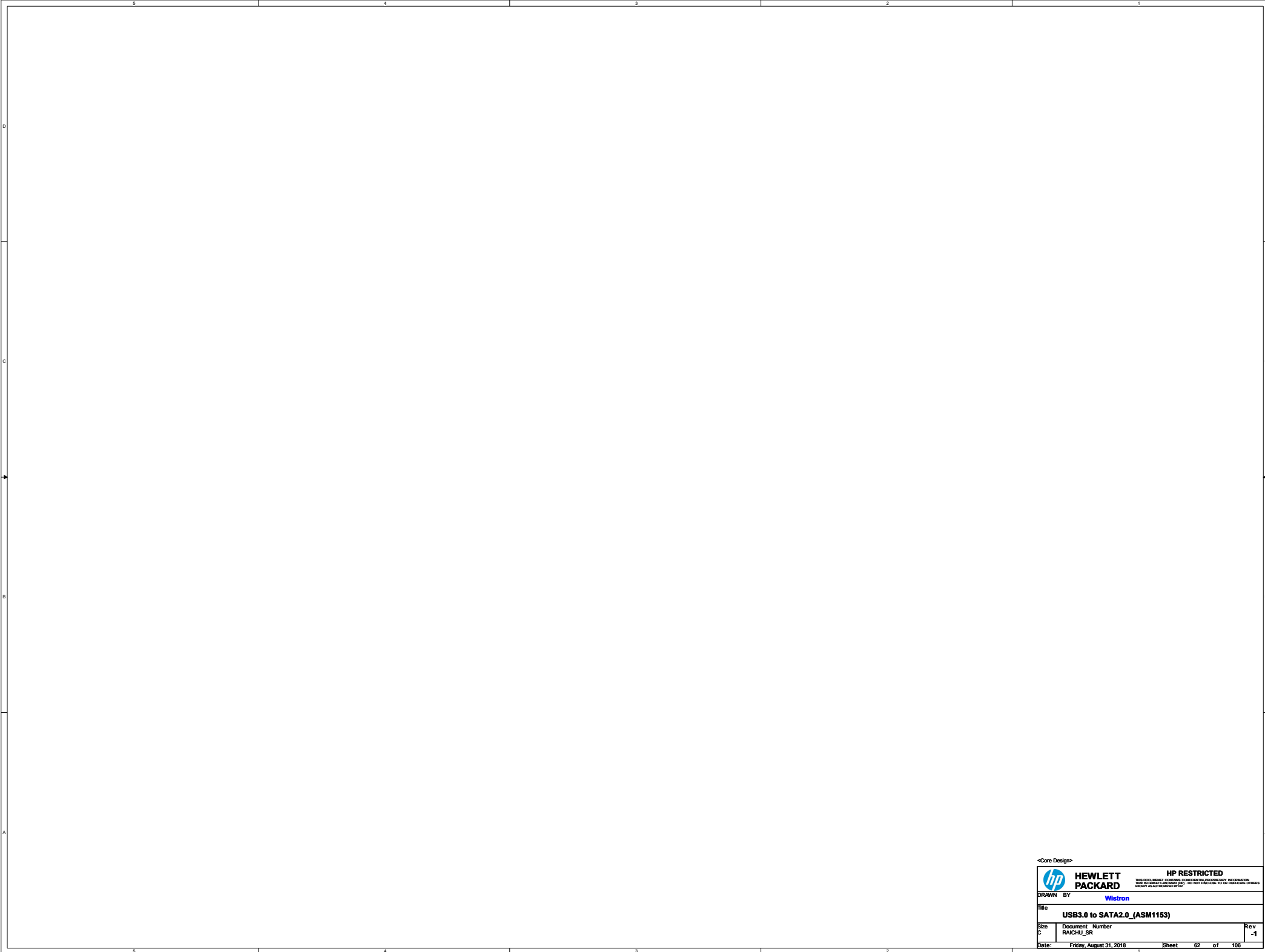
SATA ODD Connector




«Core Design»

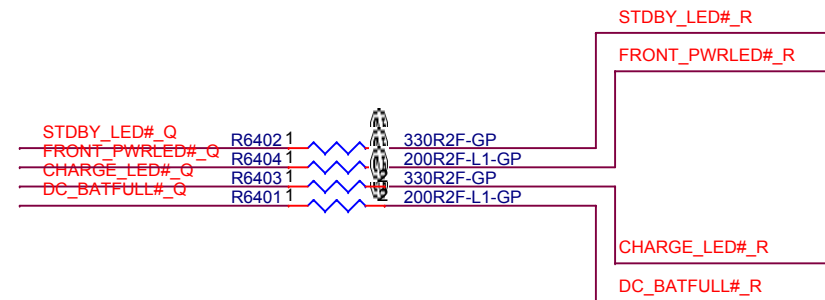
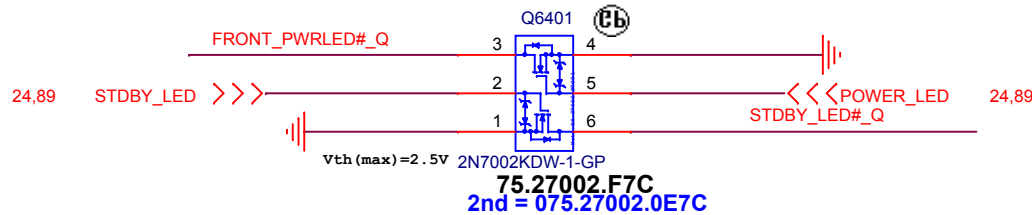
緯創資通 Wistron Corporation
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EXT IO (RSVD)			
Size	Document	Number	Rev
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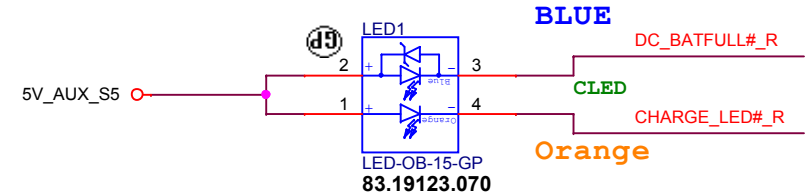
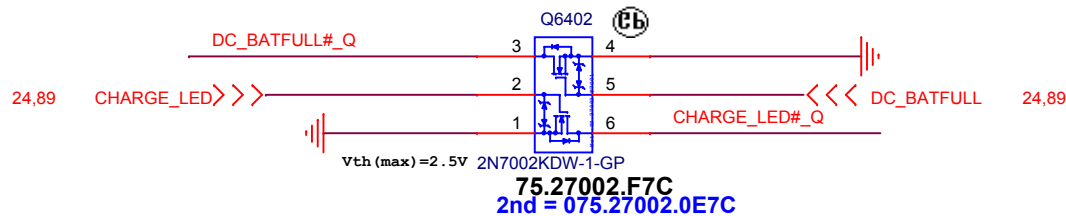
<Core Design>		HP RESTRICTED	
		HEWLETT PACKARD	
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DRAWN BY		Wistron	
Title		USB3.0 to SATA2.0 (ASM1153)	
Size	Document Number	Rev	
C	RAICHU_SR	-1	
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Power button LED

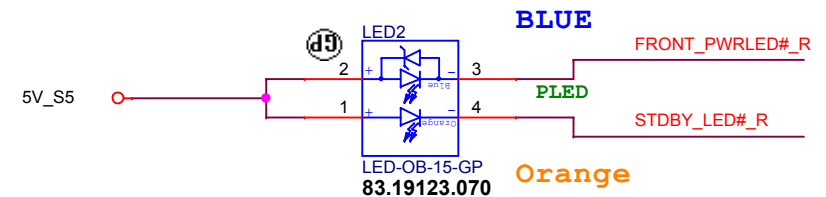
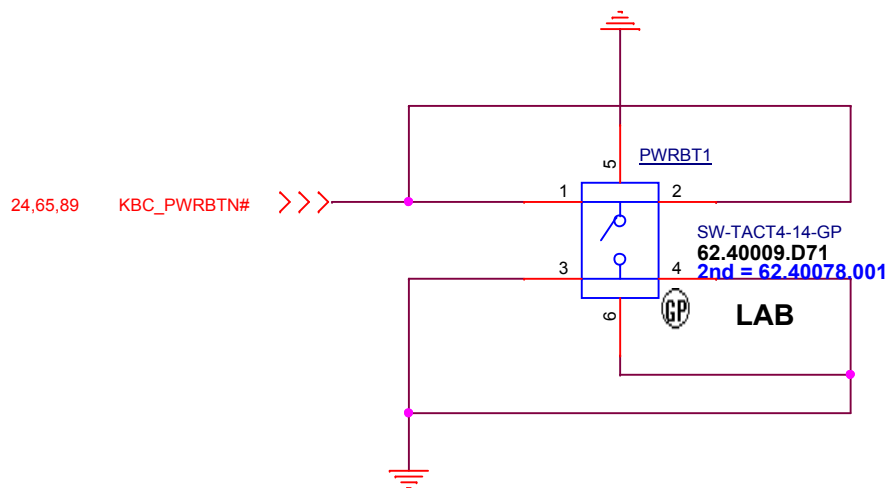


Power STDBY_LED

Battery LED2 (DC_BATFULL)



Battery LED1 (CHARGE)



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Wistron Corporation

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Title

LED And Hall Sensor

Size

A4

Document Number

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Rev

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Sheet 64 of 6

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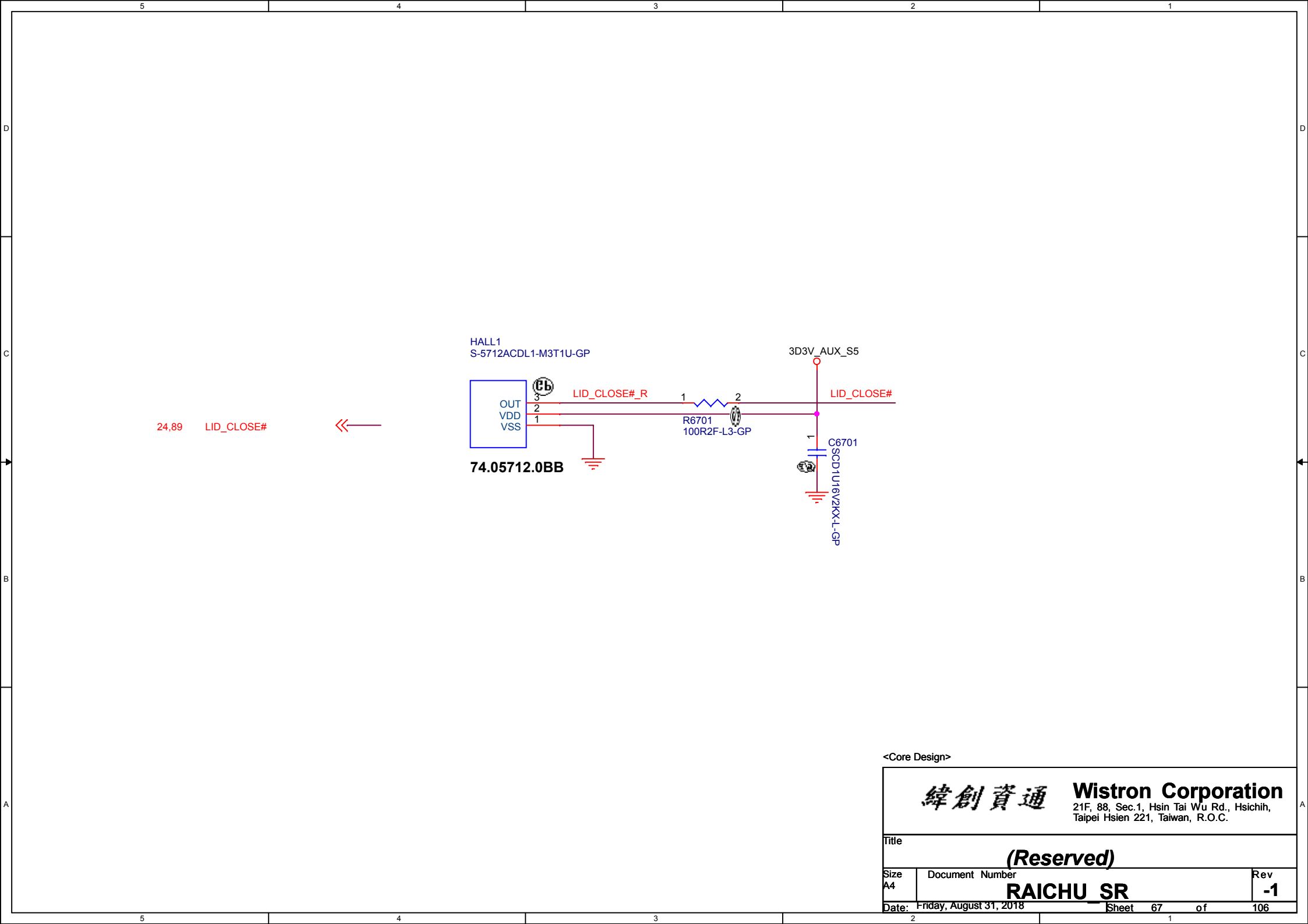
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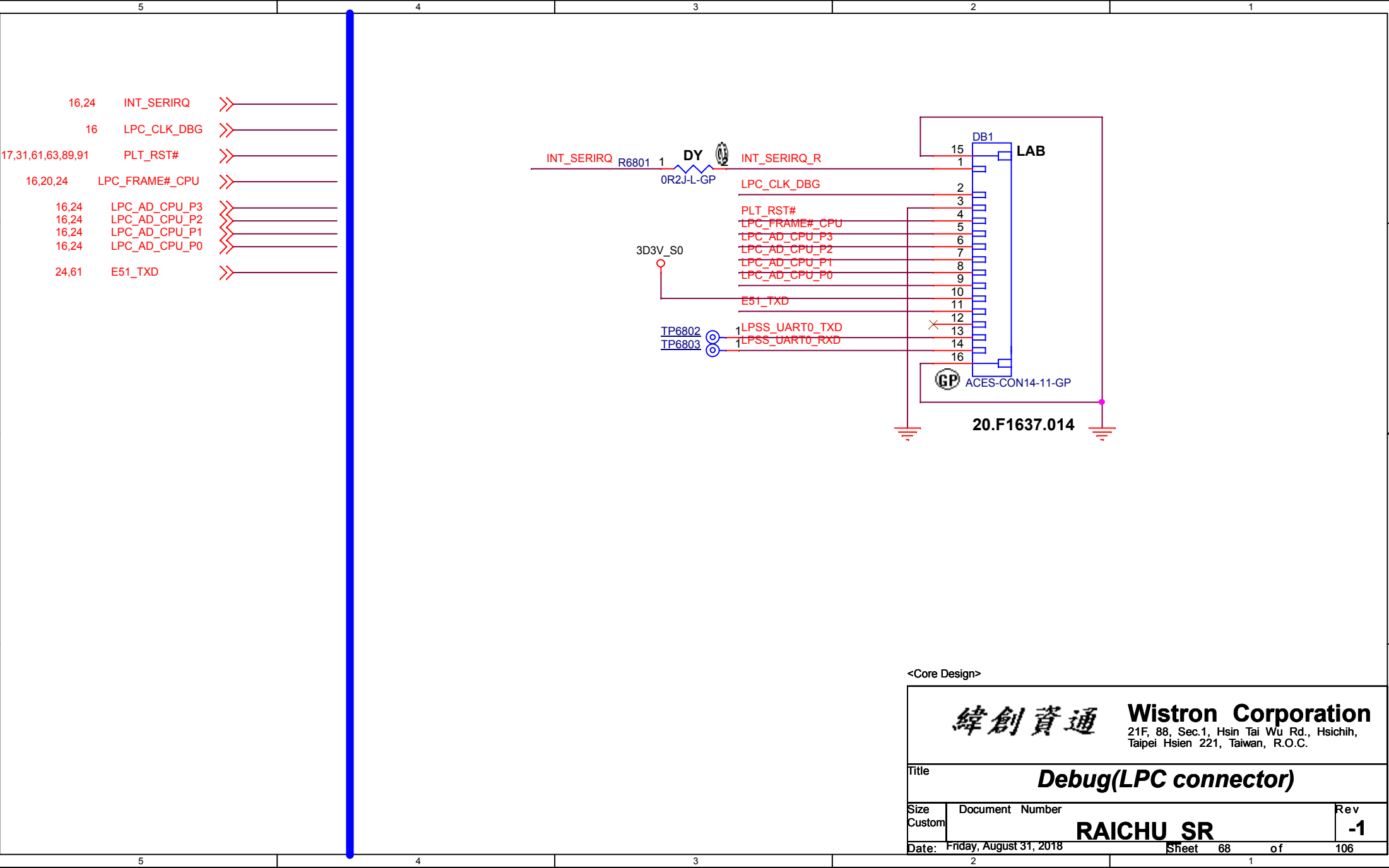
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Title <div>IO Board Conn(LED/USB/CR)</div>		
Size <div>A</div>	Document Number <div>RAICHU_SR</div>	Rev <div>-1</div>
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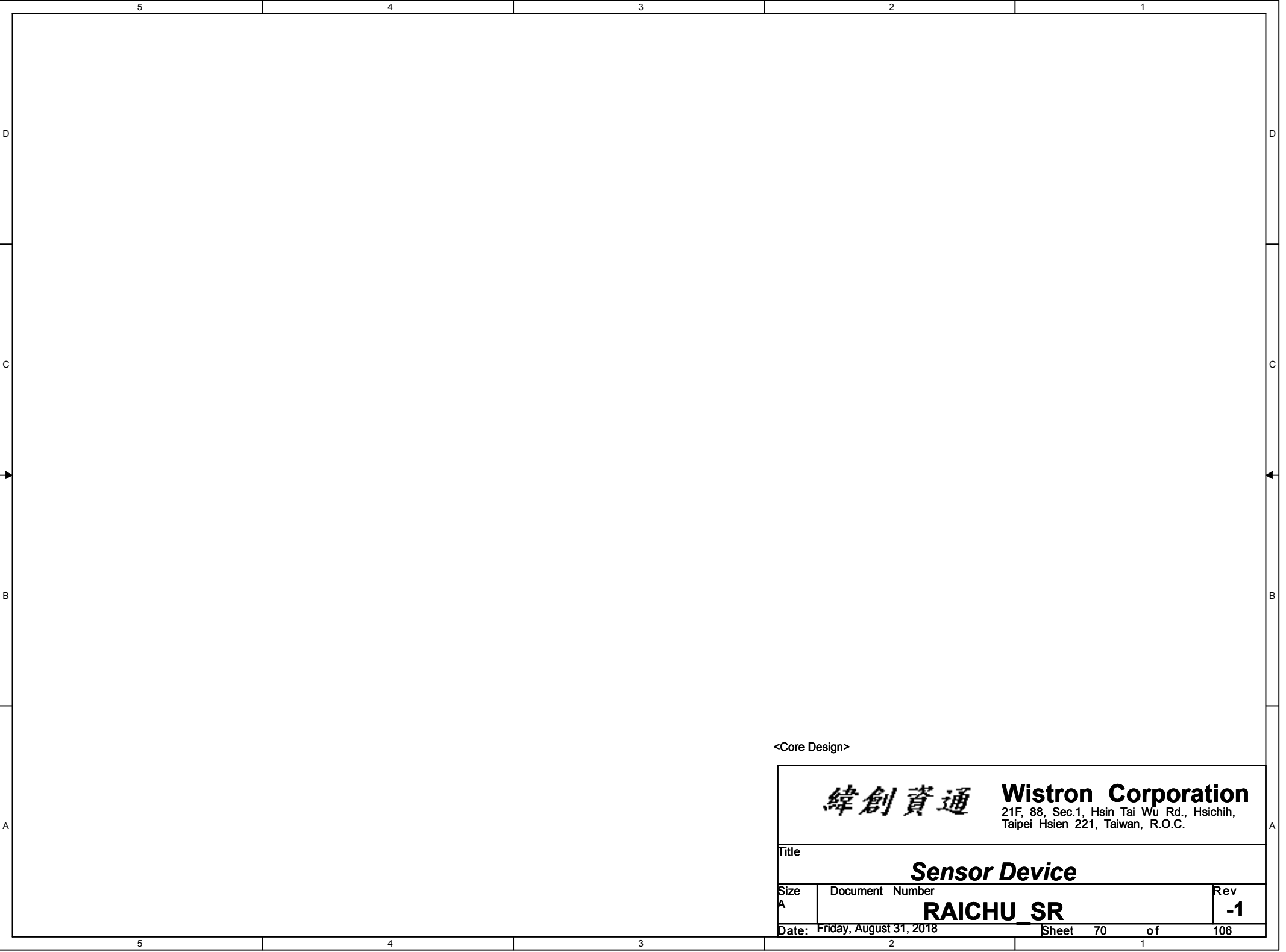
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Title					
<i>Debug(LPC connector)</i>					
Size	Document Number		Rev		
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Title <div>G Sensor (Reserved)</div>		
Size <div>A4</div>	Document Number <div>RAICHU_SR</div>	Rev <div>-1</div>
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Title <div>Sensor Device</div>		
Size <div>A</div>	Document Number <div>RAICHU_SR</div>	Rev <div>-1</div>
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Title <div>EXT IO (RSVD)</div>		
Size <div>A4</div>	Document Number <div>RAICHU SR</div>	Rev <div>-1</div>
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Title <div>EXT IO (RSVD)</div>		
Size <div>A4</div>	Document Number <div>RAICHU SR</div>	Rev <div>-1</div>
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Size <div>A4</div>	Document Number <div>RAICHU SR</div>	Rev <div>-1</div>
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Title <div>(Reserved)</div>		
Size <div>A4</div>	Document Number <div>RAICHU SR</div>	Rev <div>-1</div>
Date: Friday, August 31, 2018		Sheet 74 of 106

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Date: Friday, August 31, 2018		Sheet 75 of 106

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Title <div>GPU (1/5) PEG</div>		
Size <div>A4</div>	Document Number <div>RAICHU_SR</div>	Rev <div>-1</div>
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Title <div>GPU (2/5) DIGITAL</div>		
Size <div>A4</div>	Document Number <div>RAICHU SR</div>	Rev <div>-1</div>
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Title <div>GPU (3/5) VRAM</div>		
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TitleGPU (4/5) GPIO		
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Title GPU (5/5) PWR/GND		
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Title VRAM1,2 (1/4)		
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Title <div>VRAM3,4 (2/4)</div>		
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Title <div>VRAM5,6 (3/4)</div>		
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Title <div>VRAM7,8 (4/4)</div>		
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Title <div>DISCRETE VGAPOWER</div>		
Size <div>A4</div>	Document Number <div>RAICHU_SR</div>	Rev <div>-1</div>
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Title <div>(Reserved)</div>		
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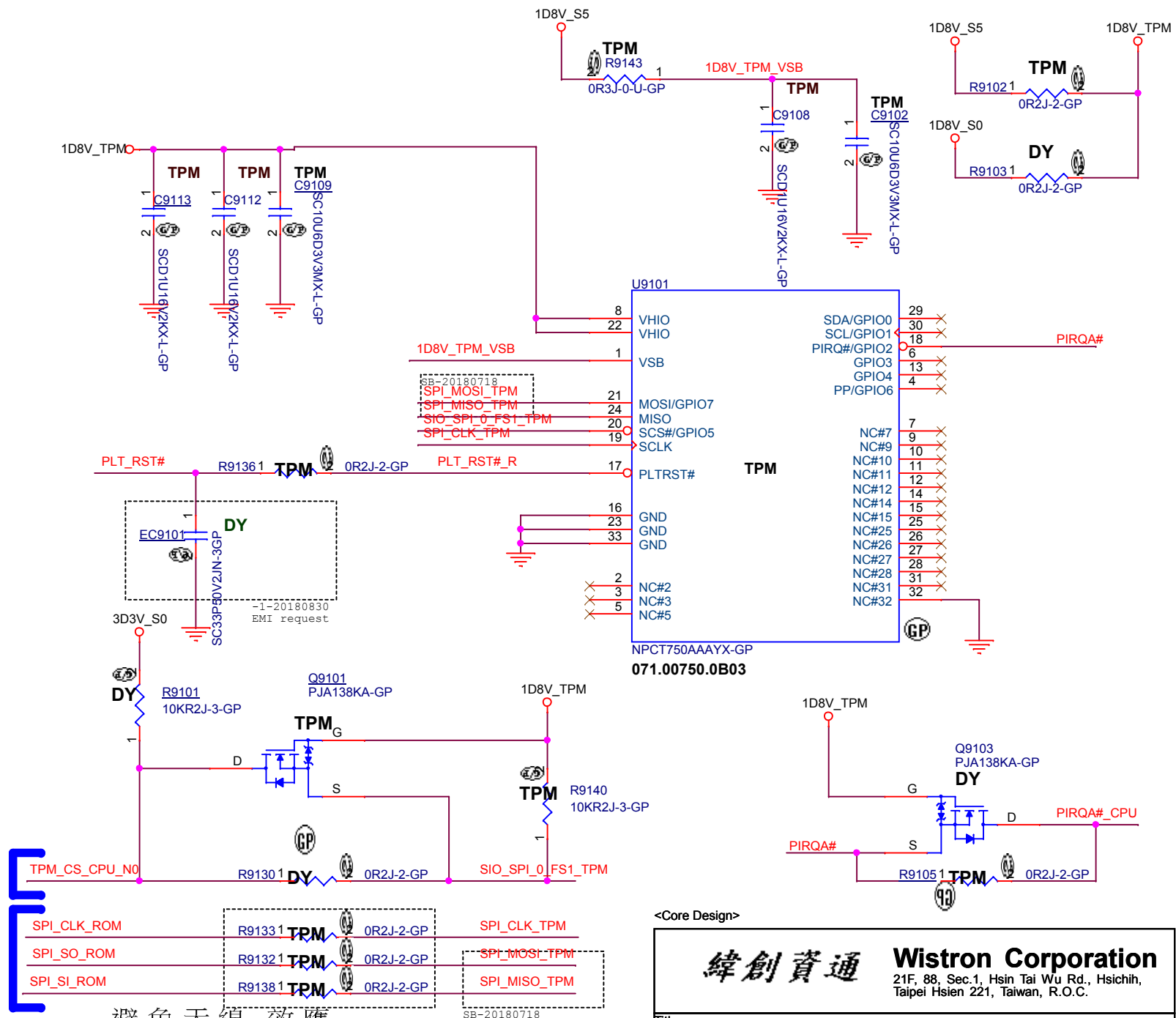
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17,31,61,63,68,89 PLT_RST#
16 TPM_CS_CPU_N0
16,24,25 SPI_CLK_ROM
16,24,25 SPI_SO_ROM
16,24,25 SPI_SI_ROM

17 PIRQA#_CPU

3.3V at CPU side

1.8V at CPU side

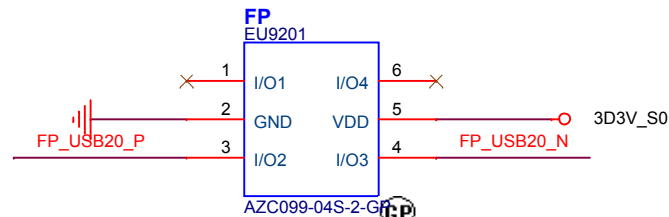


避免天線效應
所以 R9133 / R9132 / R9138
不修改成 sh ortpd

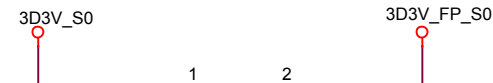
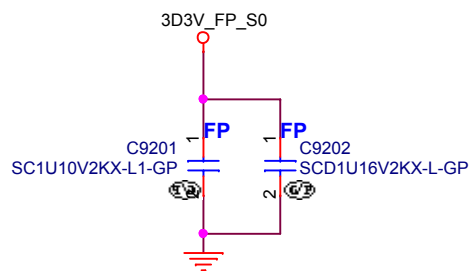
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Title INT IO (TPM)		
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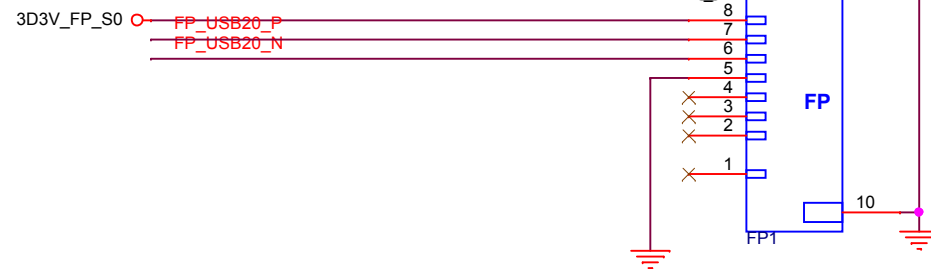
16 FP_USB20_P
16 FP_USB20_N



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2nd = 075.01256.007C
3rd = 75.08902.07C



R9201
0R0805-PAD-1-GP-U



20.K0767.008
2nd = 020.K0376.0008

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Title

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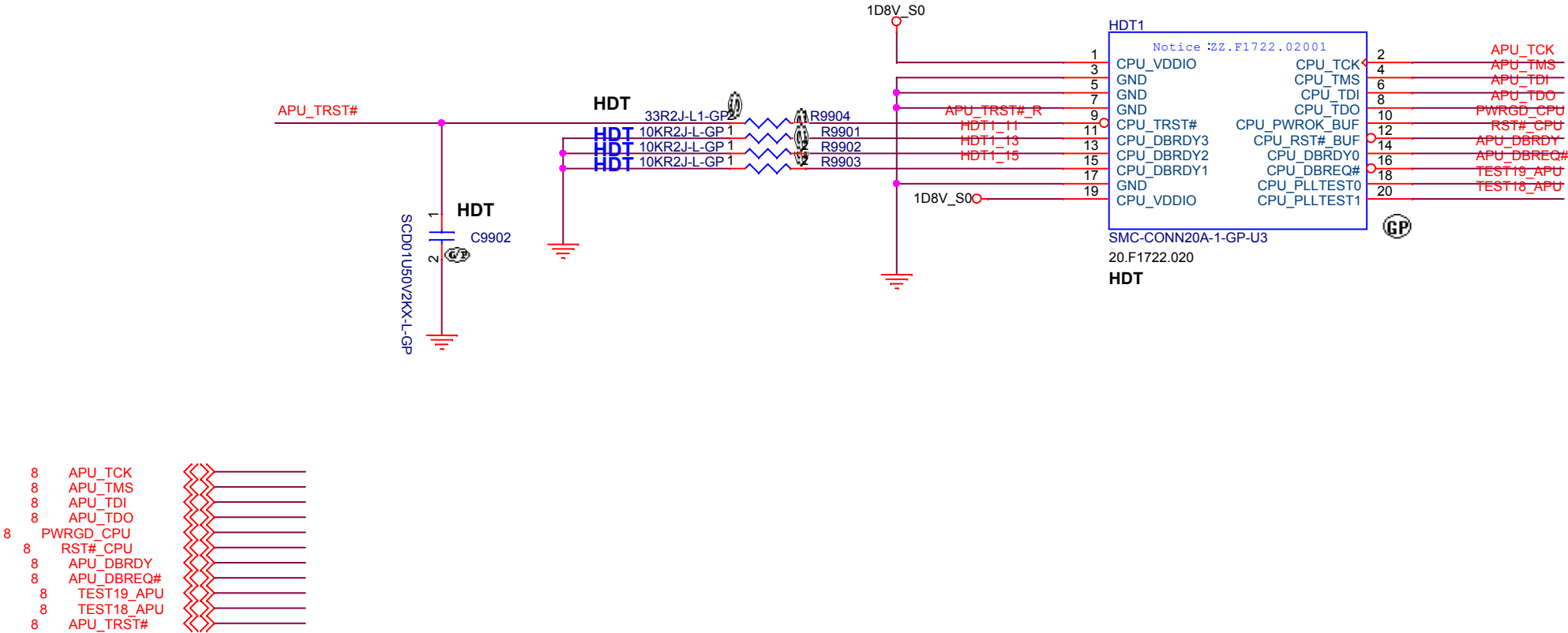
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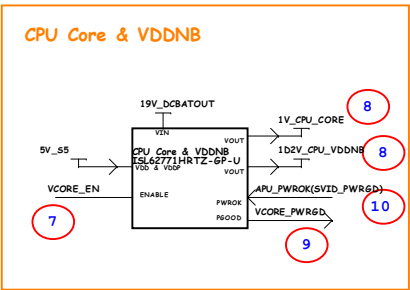
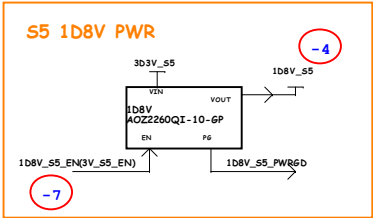
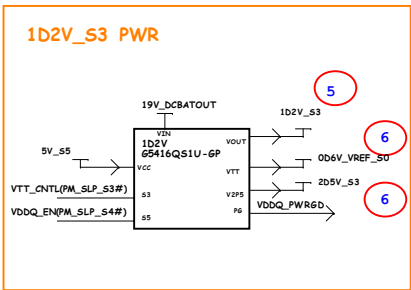
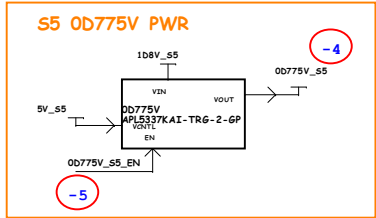
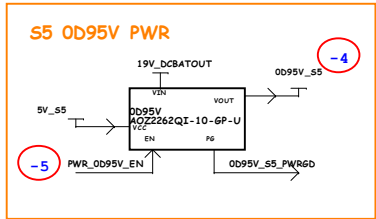
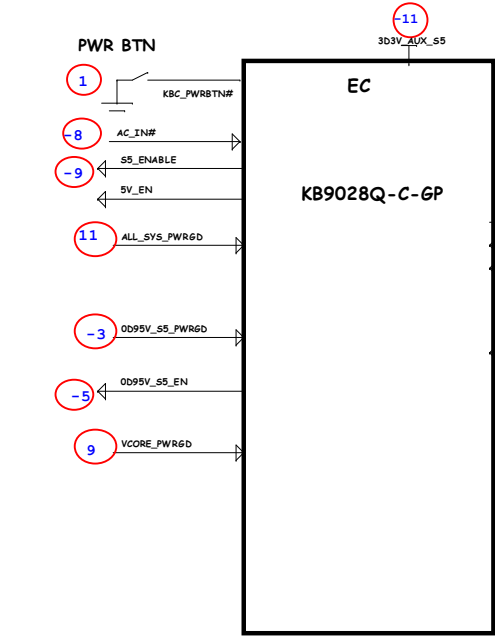
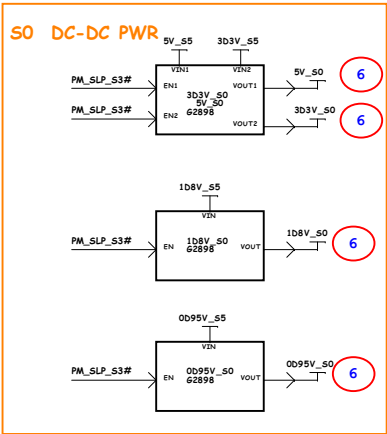
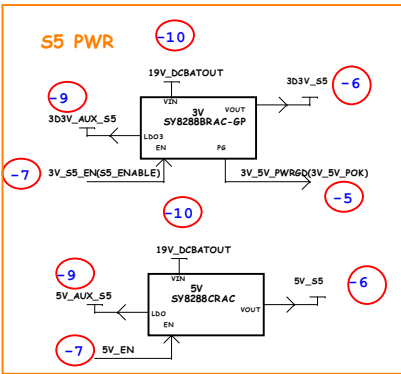
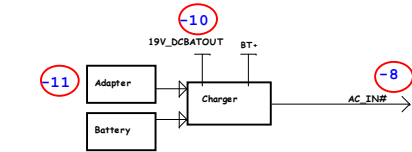
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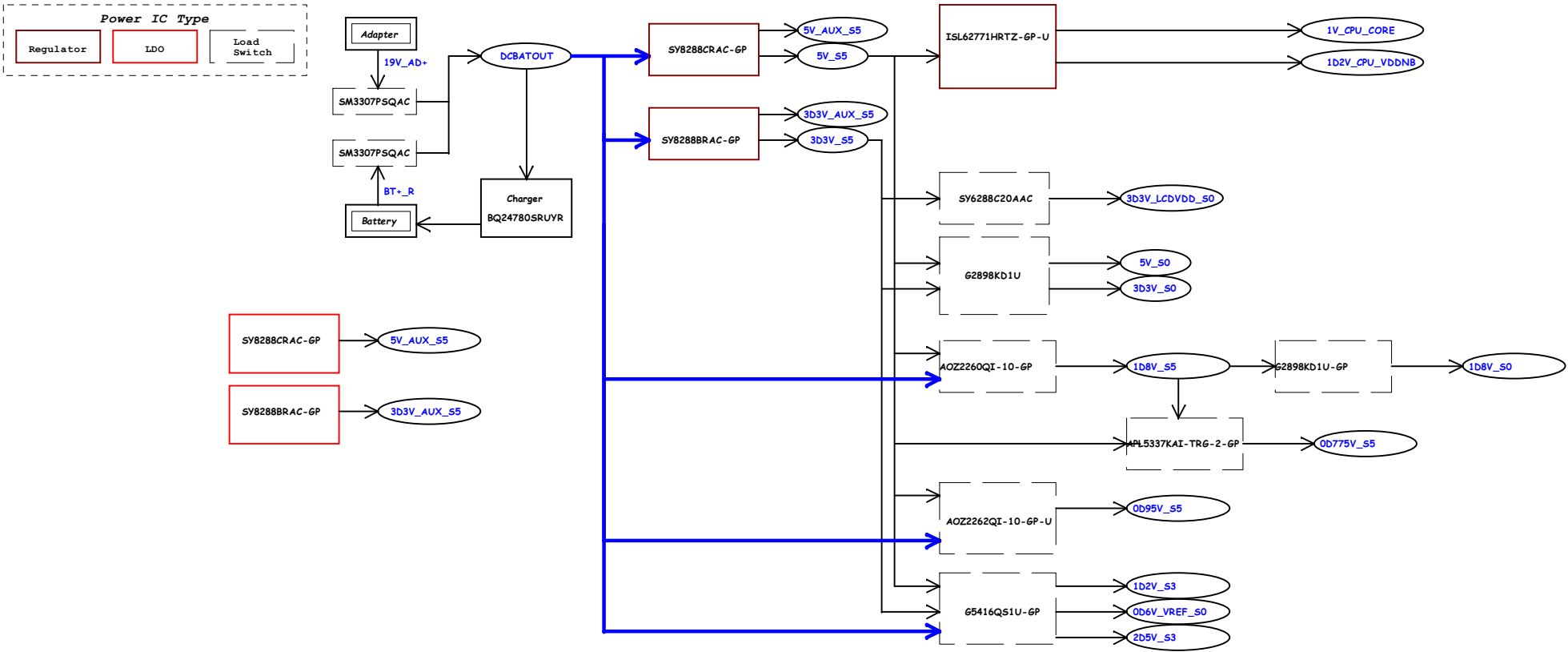
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Power Sequence Block Diagram

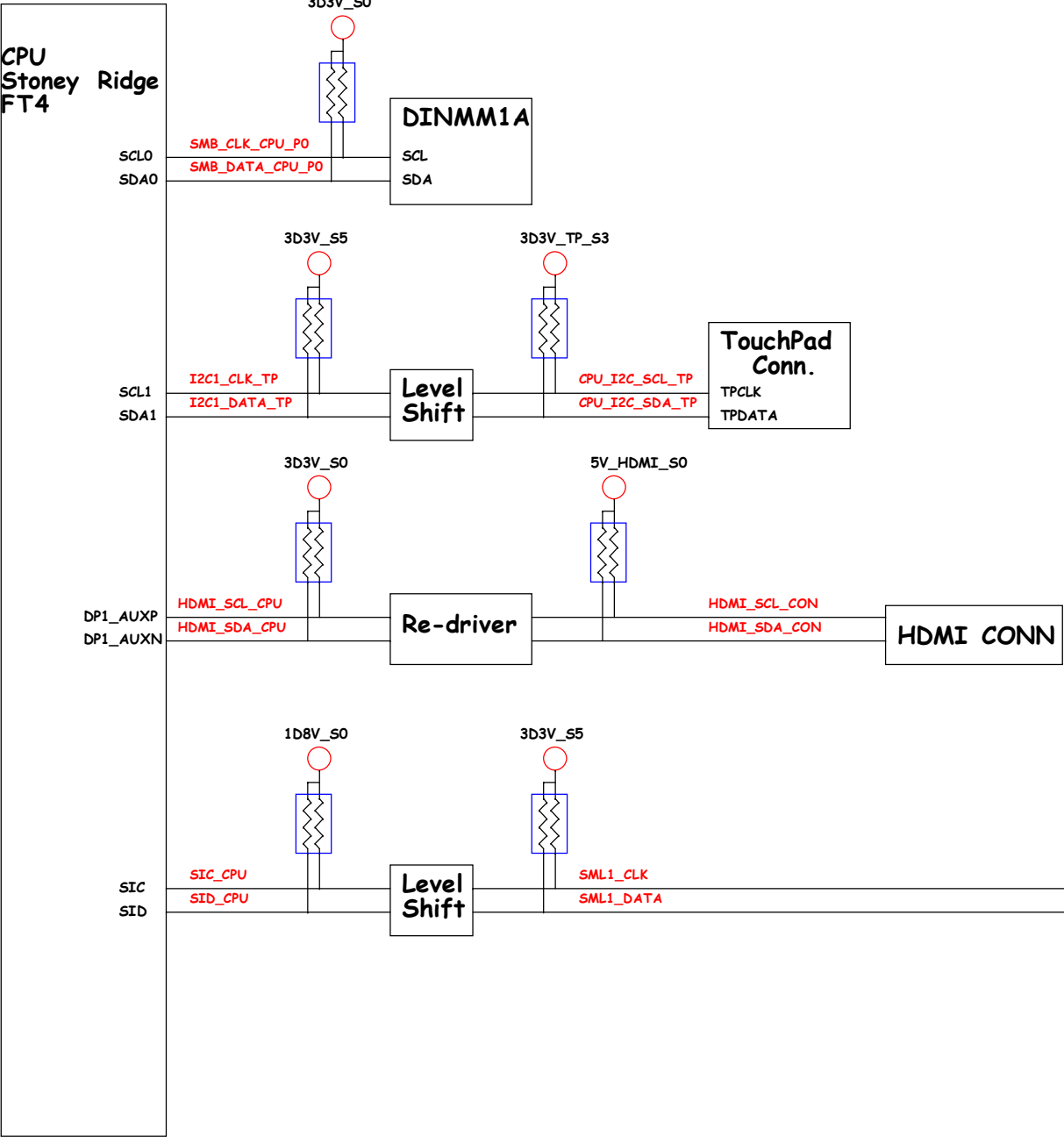


EC power on
ON1_1D8V->High
S5_ENABLE->High
0D95V_S5_EN->High
0D95V_S5_PWRGD->High
RSMRST#KBC->High

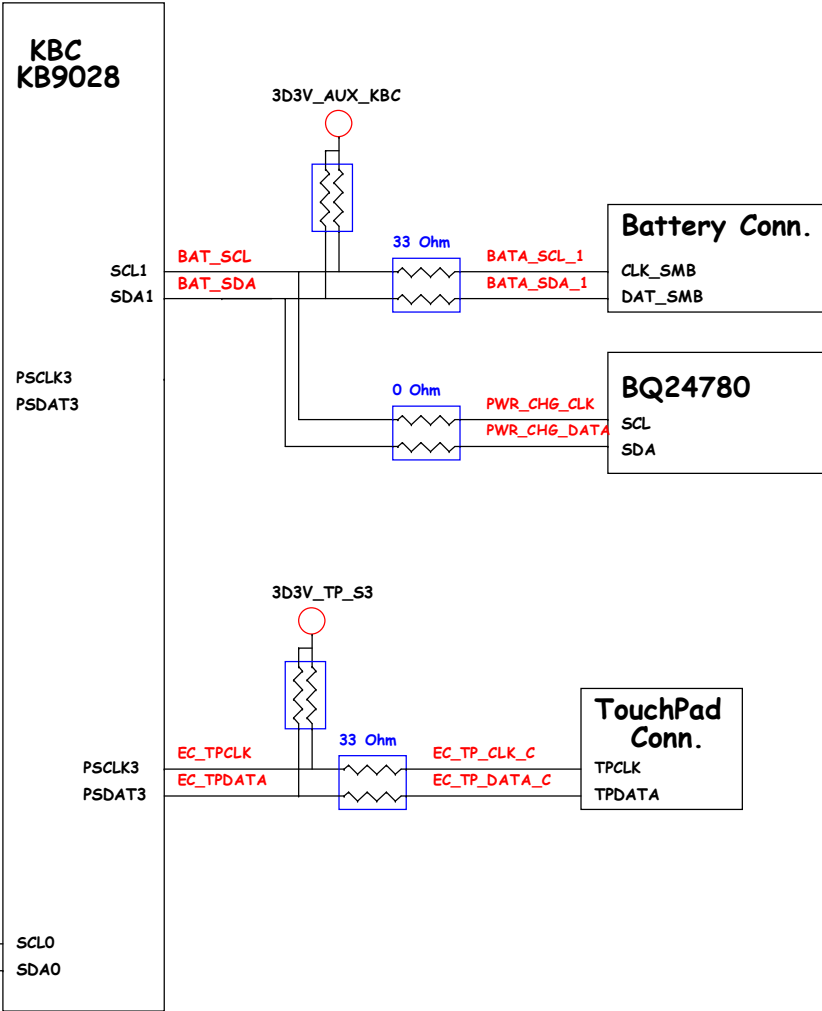
Stoney Ridge FT4 Power BLOCK DIAGRAM



PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title <div>THERMAL/AUDIO BLOCK DIAGRAM</div>		
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